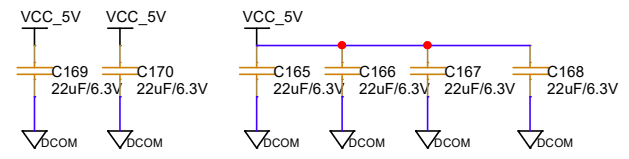
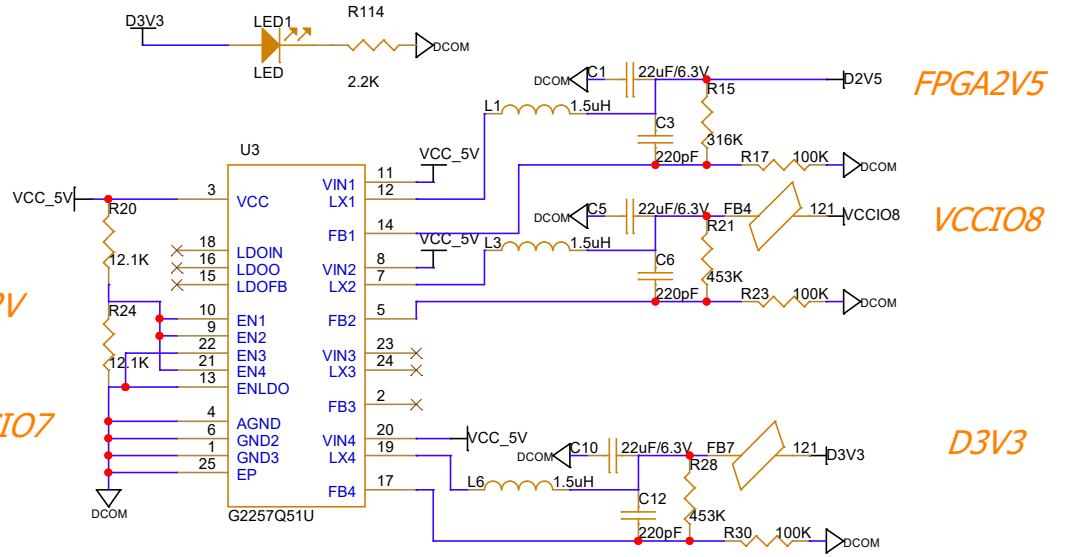
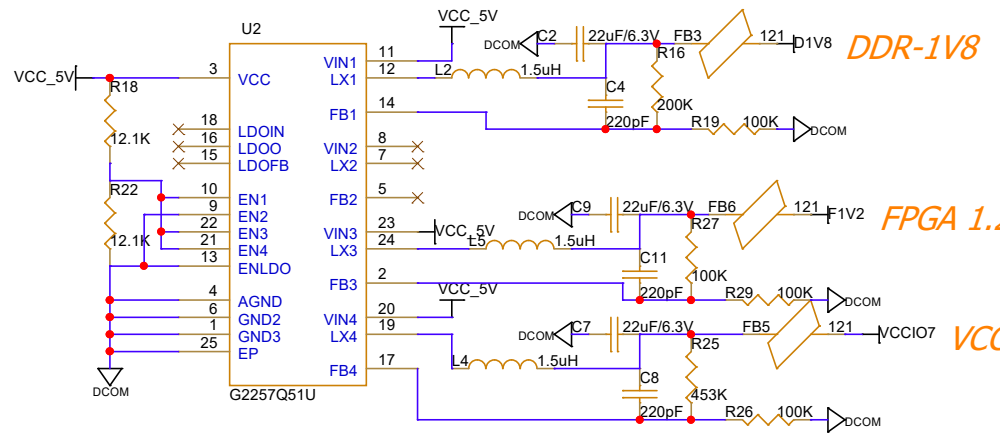
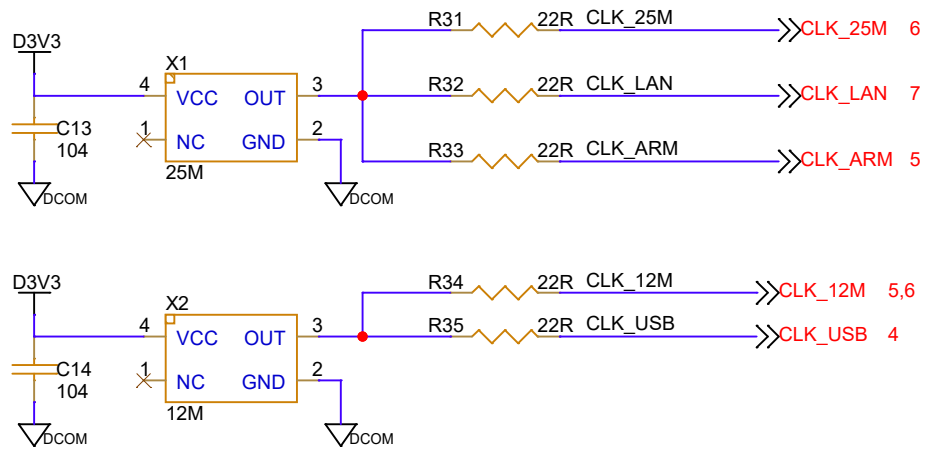


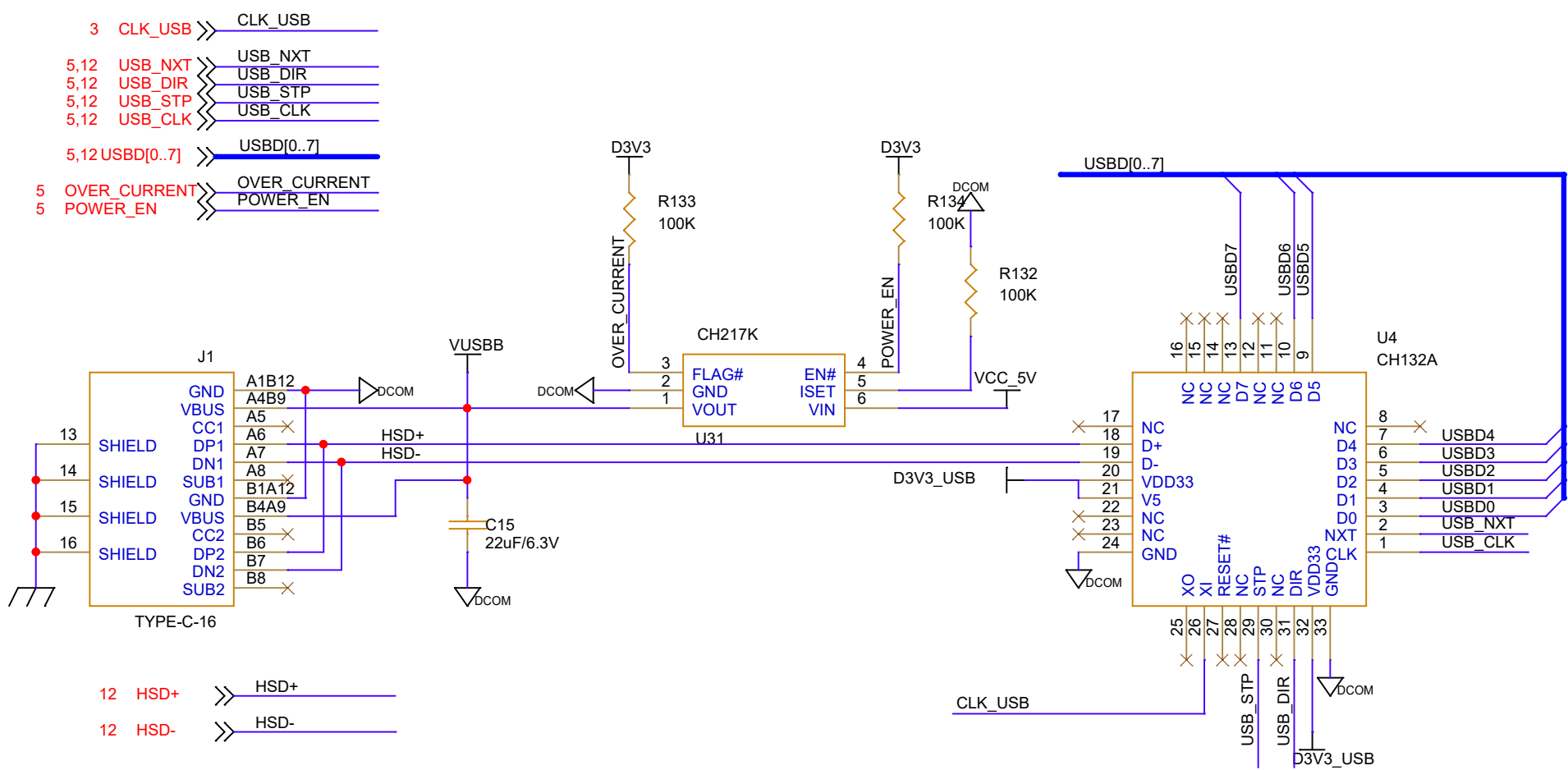
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阻值1780R--电流1.17A;  
阻值4420R--电流0.49A;



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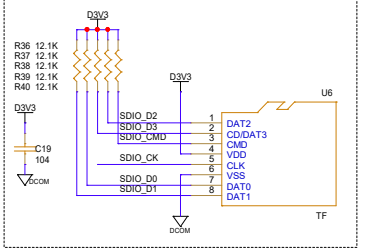


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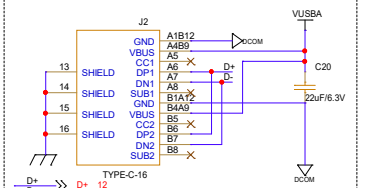


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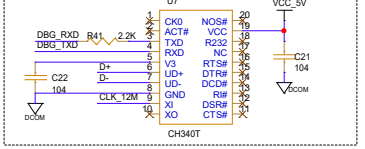
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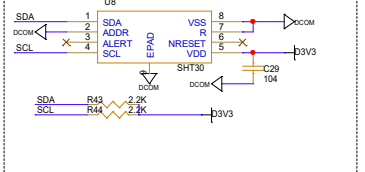
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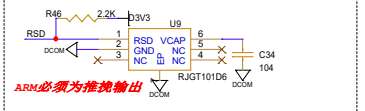
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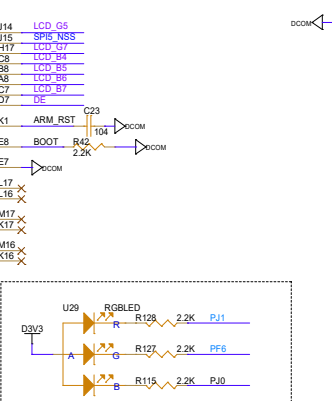
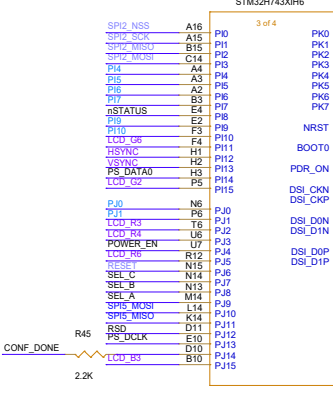
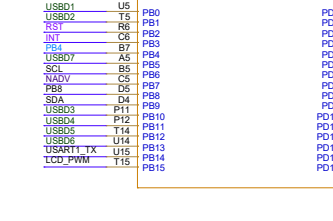
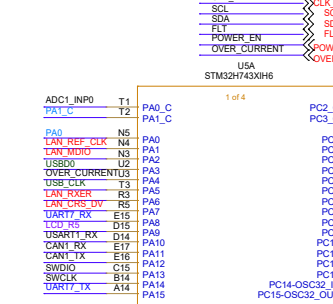
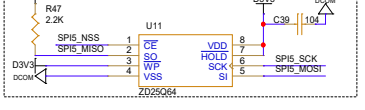
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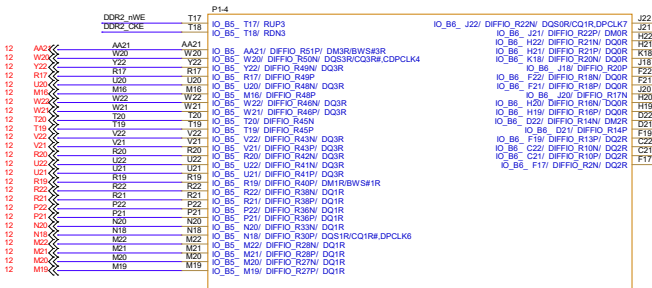


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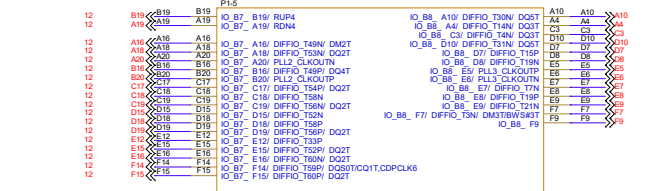


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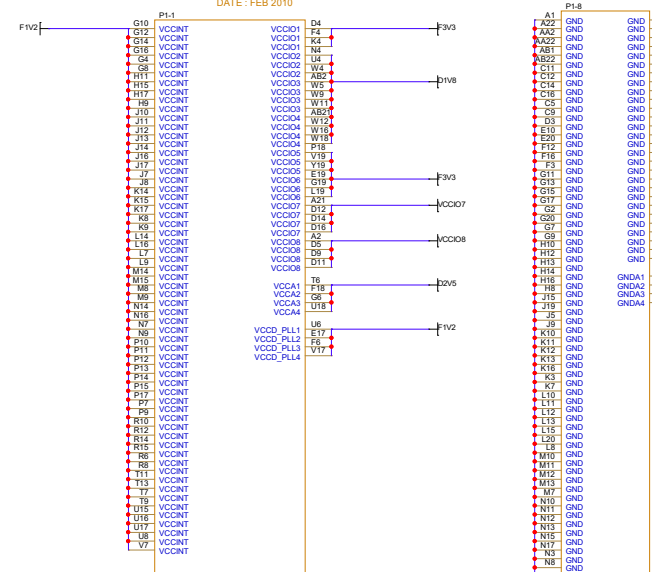




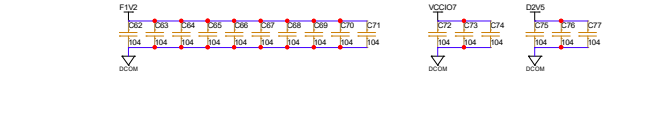
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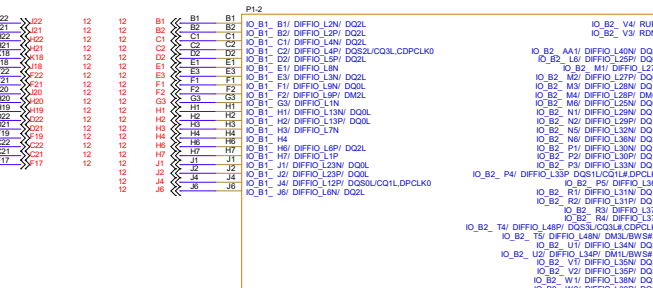
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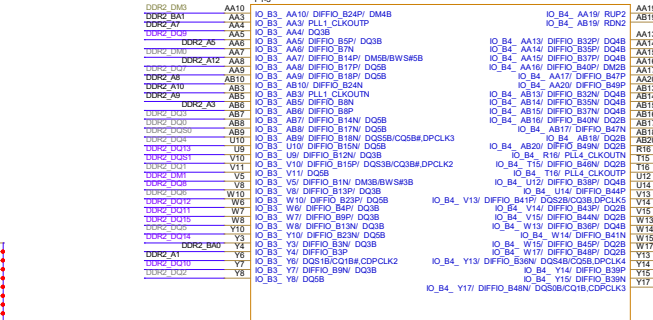
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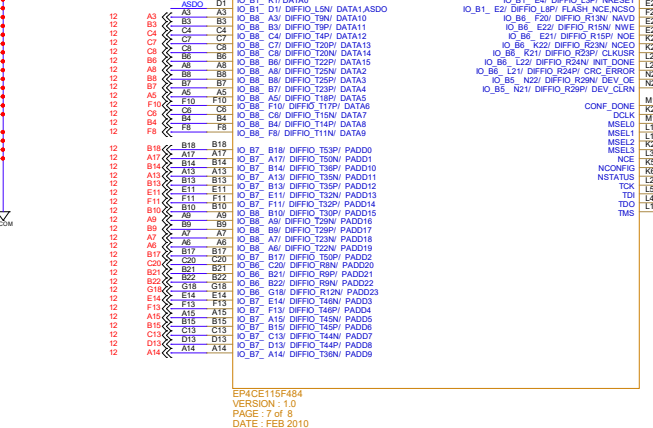
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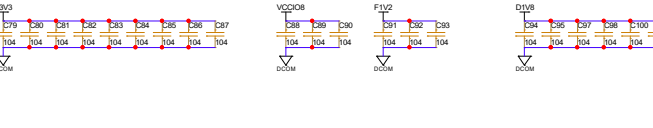
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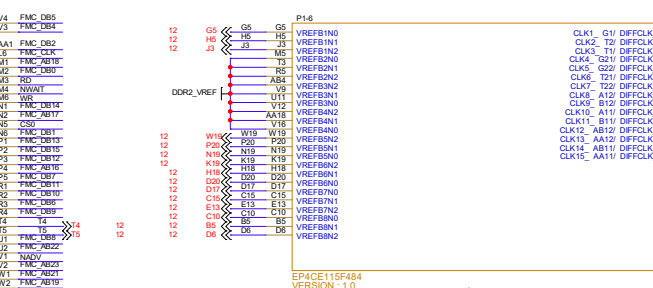
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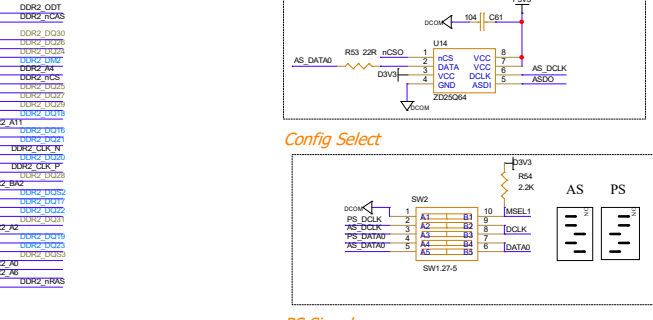
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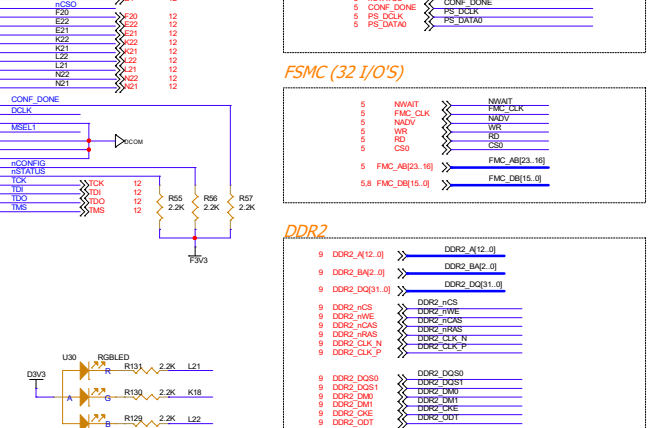
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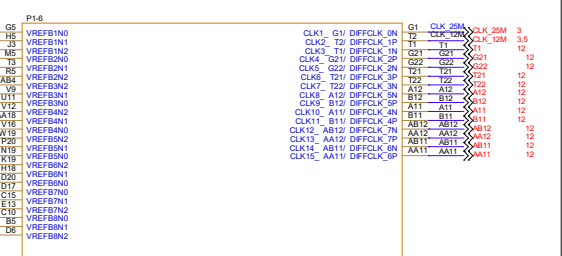
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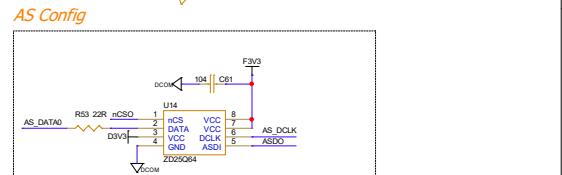
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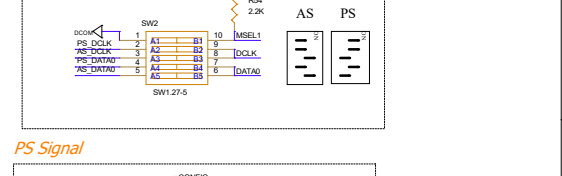
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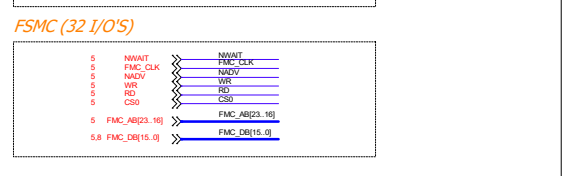
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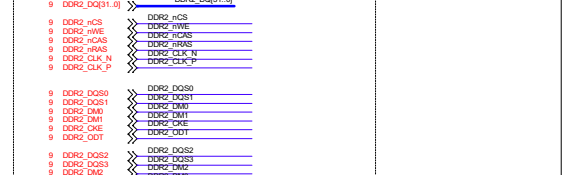
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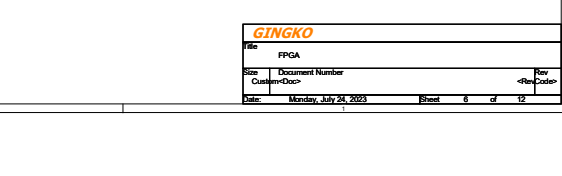
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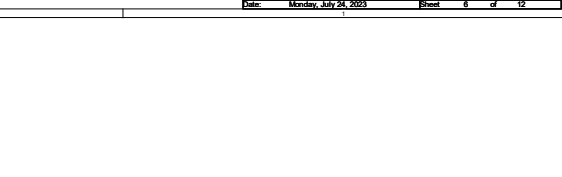
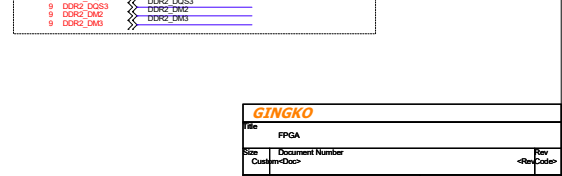
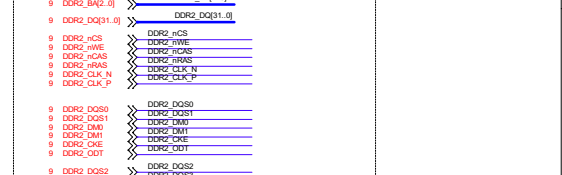
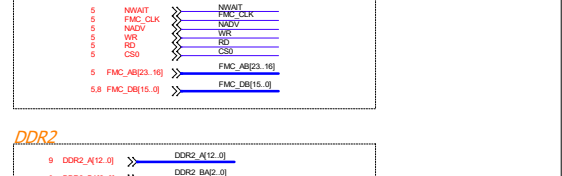
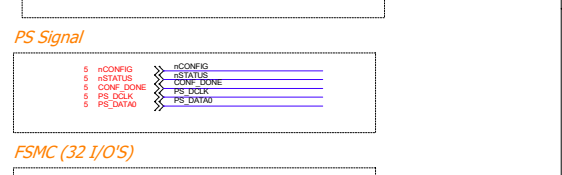
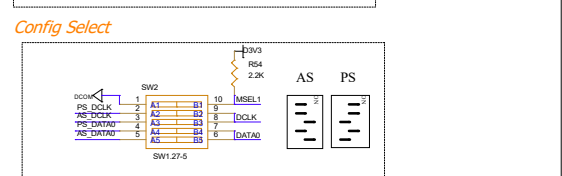
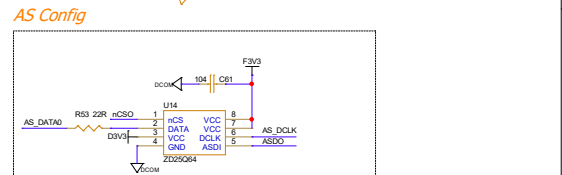
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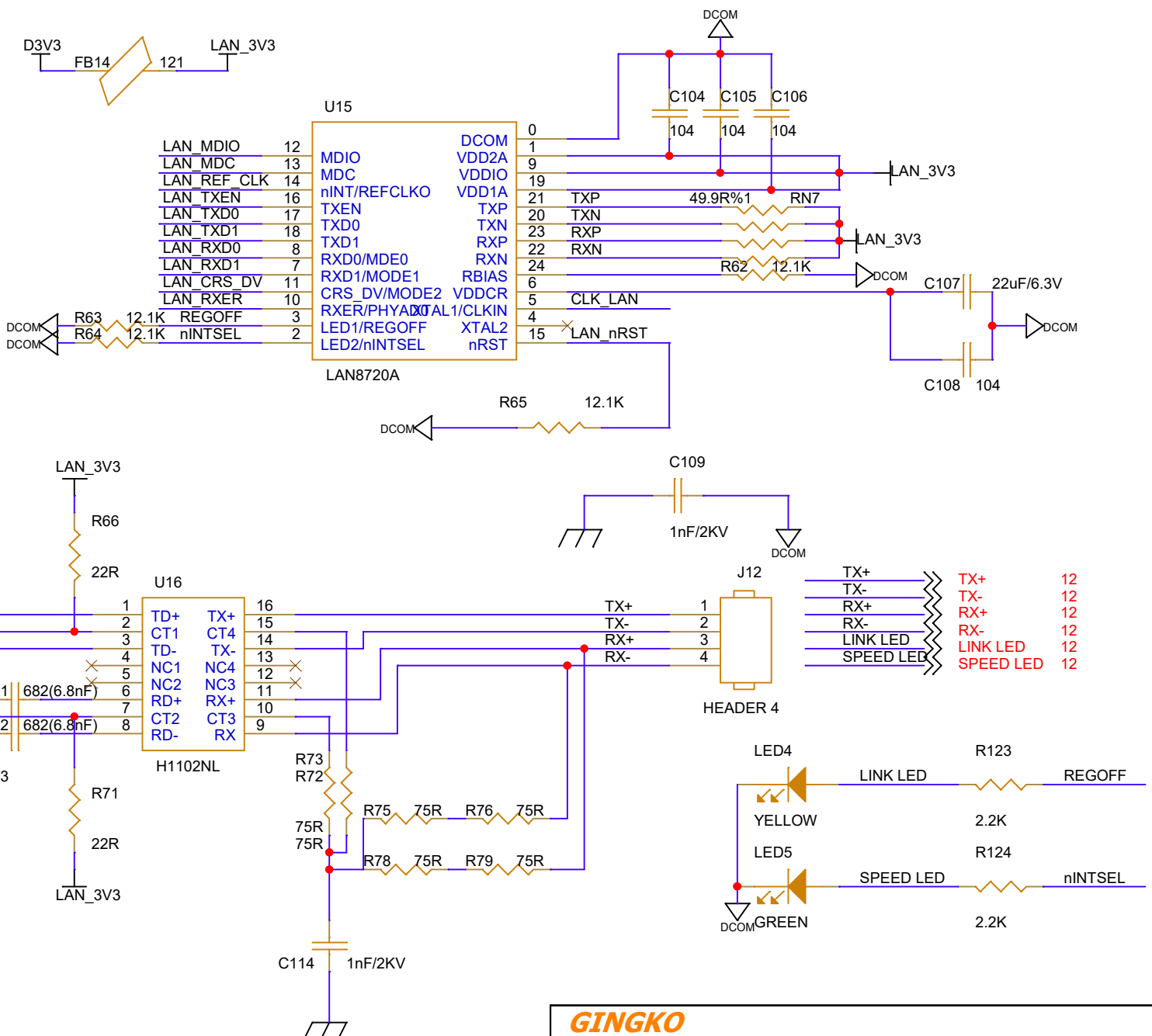
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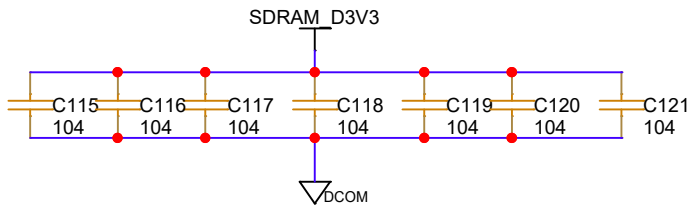
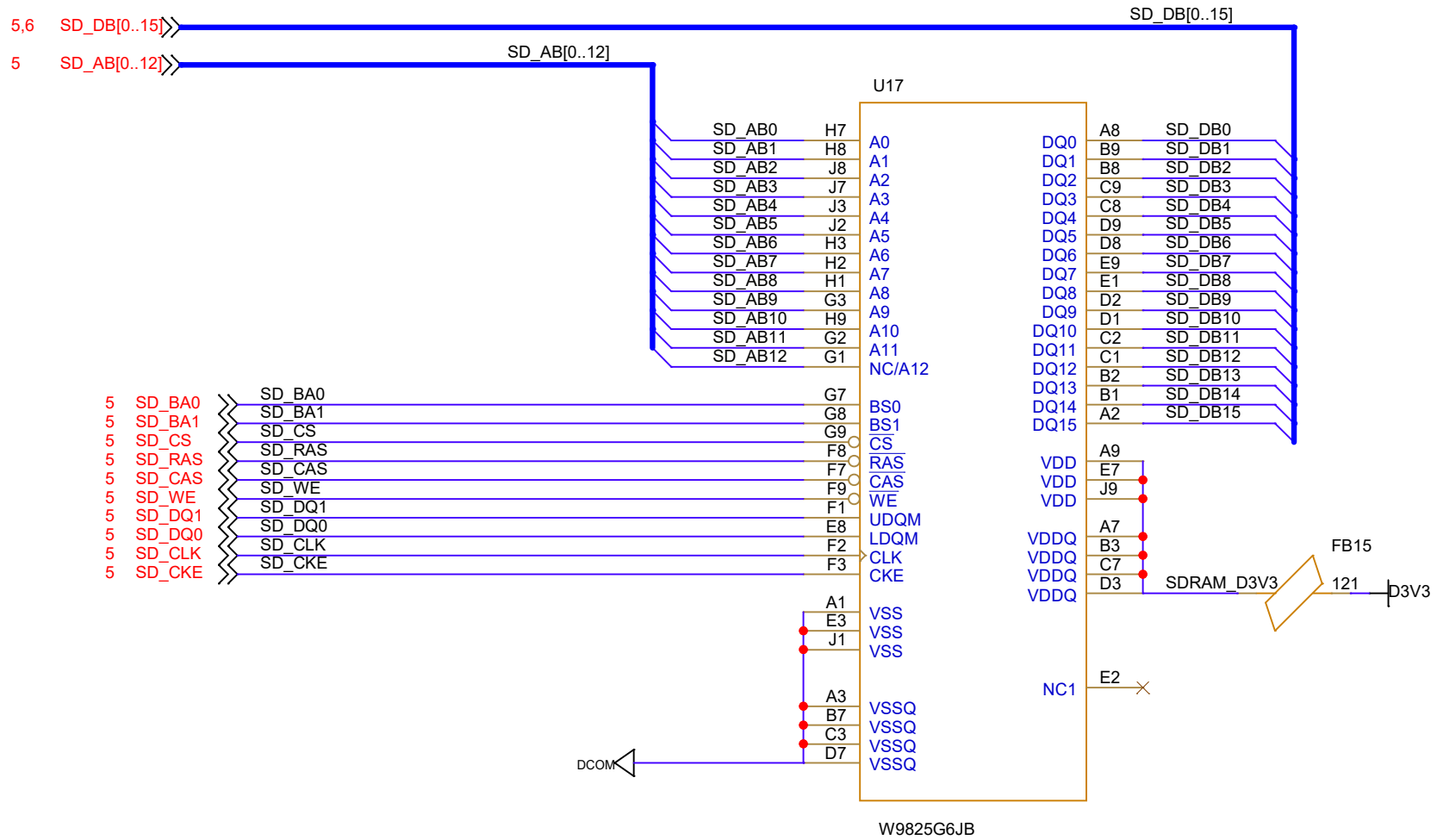
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- 5,12 LAN\_nRST >>> LAN\_nRST
- 5,12 LAN\_REF\_CLK >>> LAN\_REF\_CLK
- 5,12 LAN\_RXER >>> LAN\_RXER
- 5,12 LAN\_CRSDV >>> LAN\_CRSDV
- 5,12 LAN\_RXD1 >>> LAN\_RXD1
- 5,12 LAN\_RXD0 >>> LAN\_RXD0
- 5,12 LAN\_TXEN >>> LAN\_TXEN
- 5,12 LAN\_TXD1 >>> LAN\_TXD1
- 5,12 LAN\_TXD0 >>> LAN\_TXD0
- 5,12 LAN\_MDC >>> LAN\_MDC
- 5,12 LAN\_MDIO >>> LAN\_MDIO
- 3 CLK\_LAN >>> CLK\_LAN

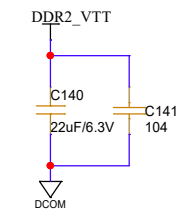
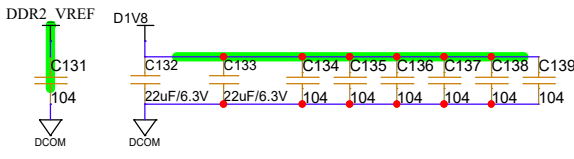
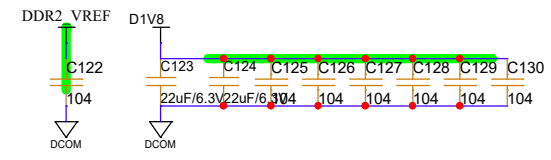
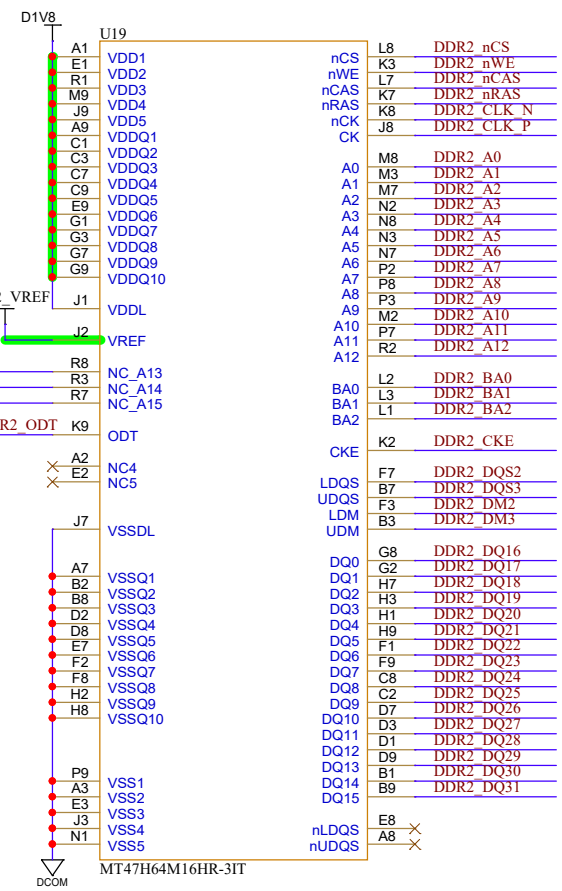
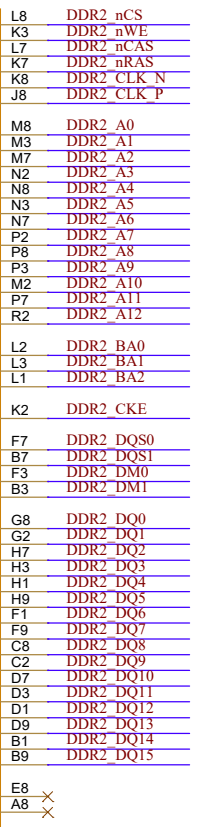
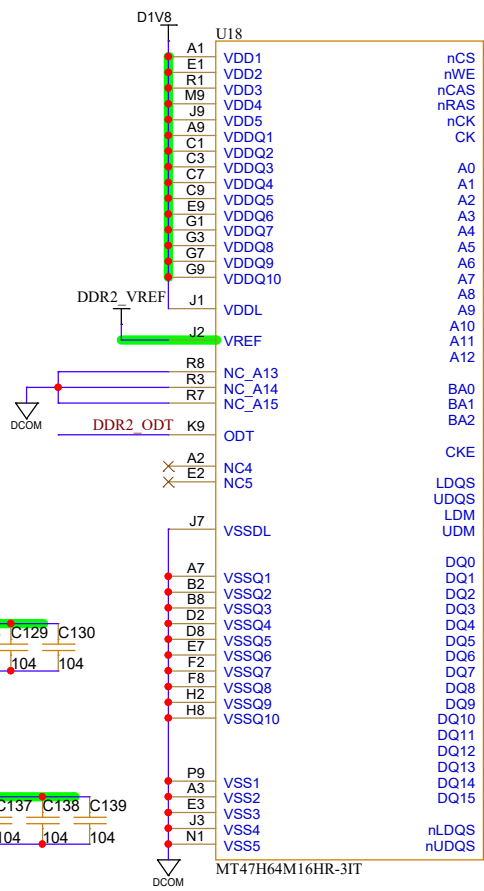
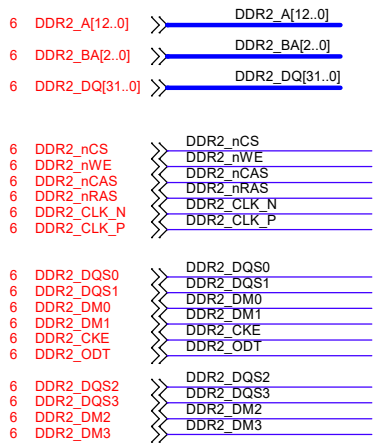


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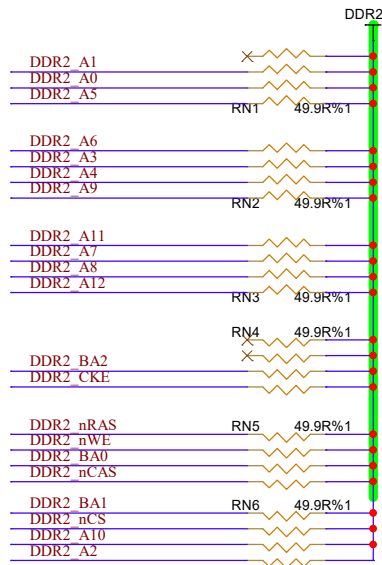
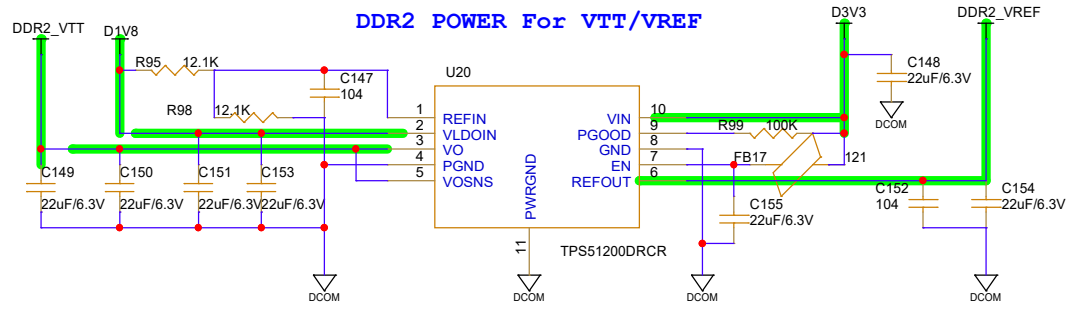


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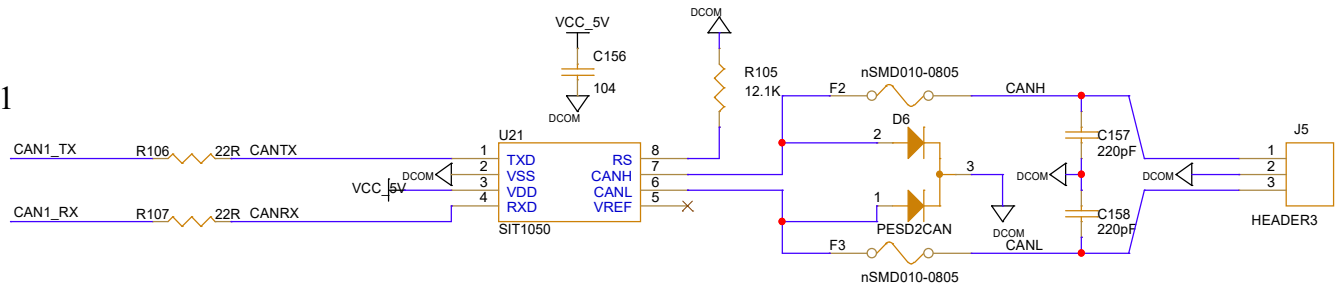


DDR2 POWER For VTT/VREF



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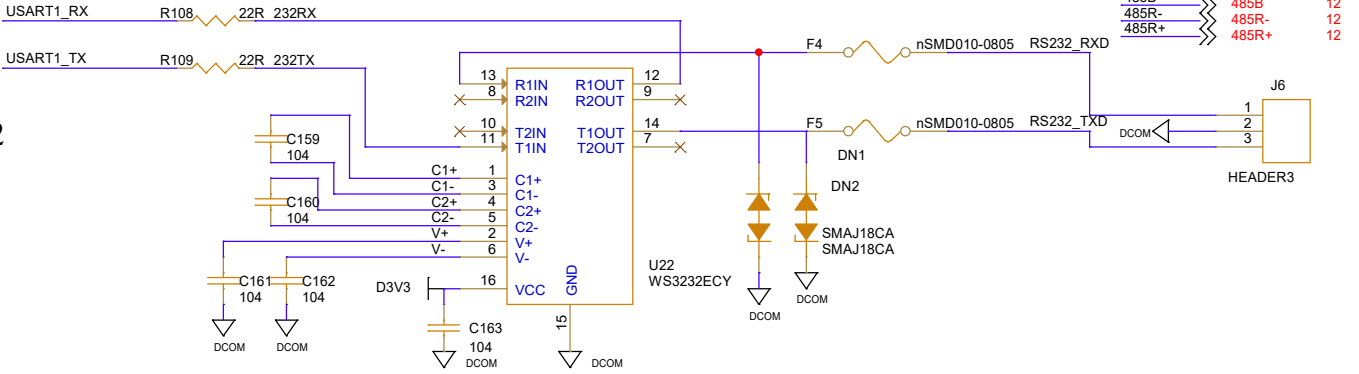
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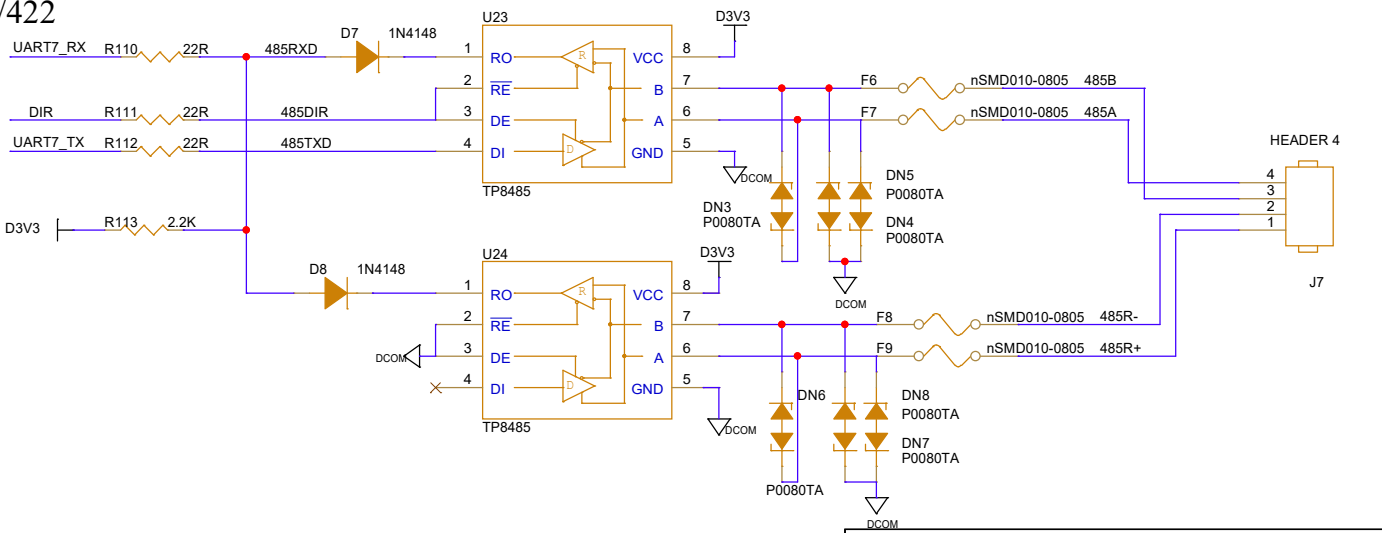
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- 5,12 USART1\_RX >> USART1\_RX
- 5,12 UART7\_TX >> UART7\_TX
- 5,12 UART7\_RX >> UART7\_RX
- 5,12 DIR >> DIR
- 5,12 CAN1\_RX >> CAN1\_RX
- 5,12 CAN1\_TX >> CAN1\_TX

- CANH >> CANH 12
- CANL >> CANL 12
- RS232\_RXD >> RS232\_RXD 12
- RS232\_TXD >> RS232\_TXD 12
- 485A >> 485A 12
- 485B >> 485B 12
- 485R- >> 485R- 12
- 485R+ >> 485R+ 12

# RS232

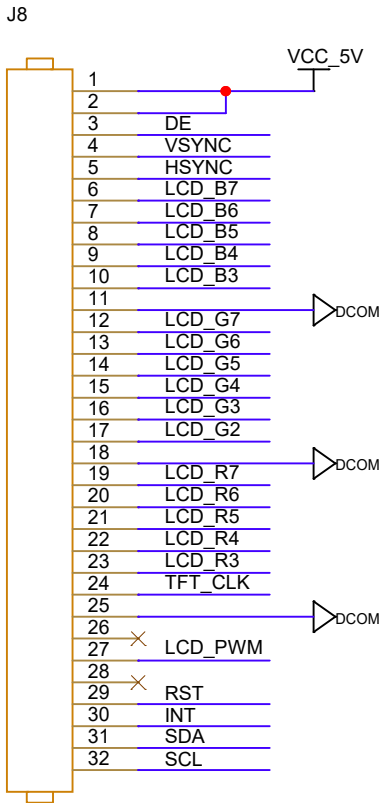
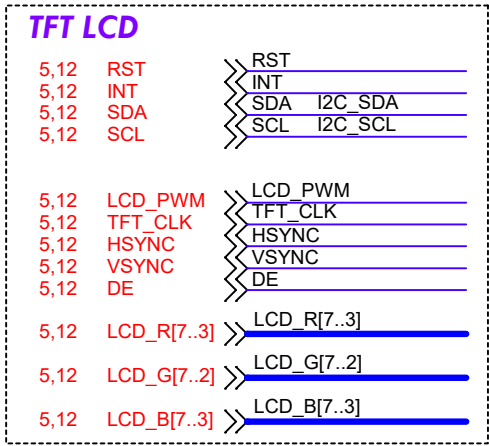


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**GINGKO**

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TFT LCD

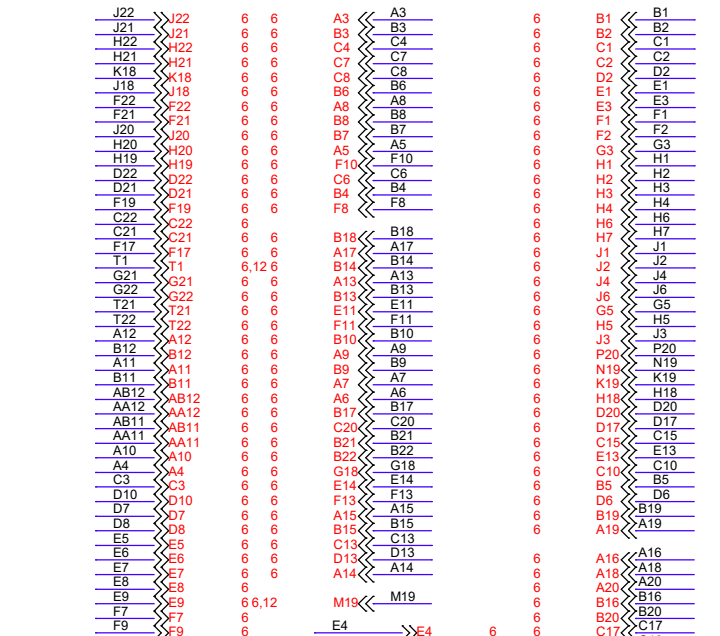
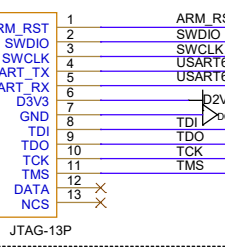
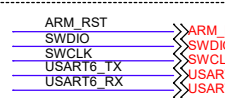
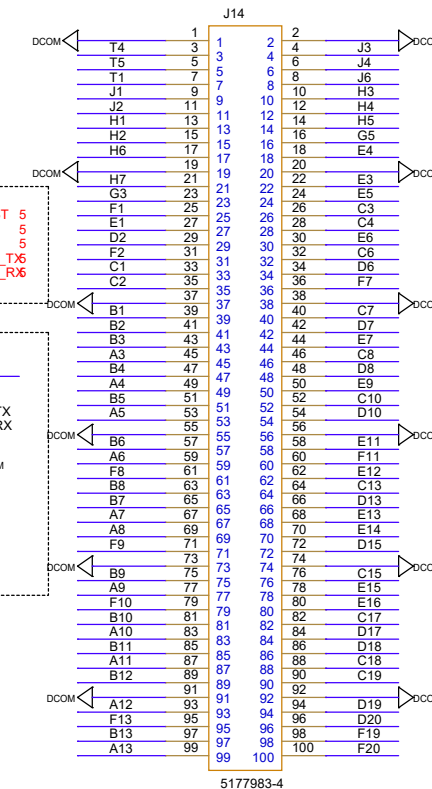
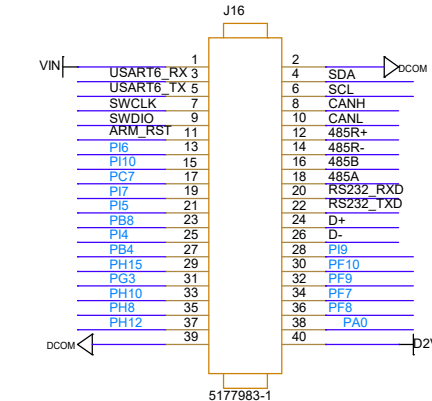
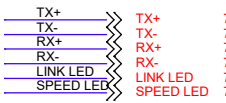
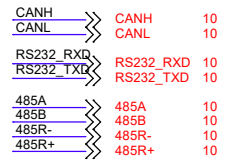
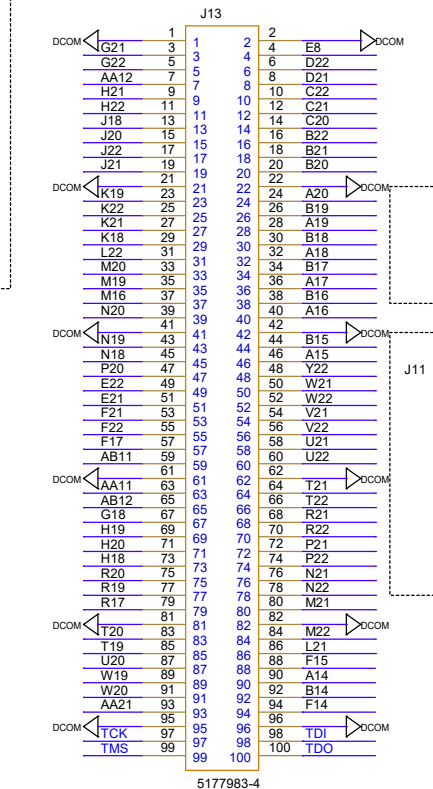
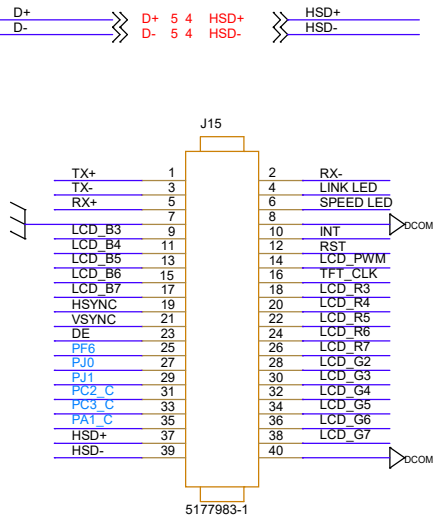
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# ARM IO 27

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PA4	PA4	5
PB4	PB4	5
PC7	PC7	5
PG3	PG3	5
PH8	PH8	5
PH10	PH10	5
PH12	PH12	5
PH15	PH15	5
PI6	PI6	5
PI7	PI7	5
PI9	PI9	5
PI10	PI10	5
PJ0	PJ0	5
PJ1	PJ1	5
PB8	PB8	5
PJ4	PJ4	5
PC2_C	PC2_C	5
PC3_C	PC3_C	5
PA1_C	PA1_C	5
PI4	PI4	5
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PF10	PF10	5
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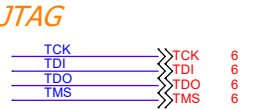
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5,11 SCL	SCL I2C_SCL
5,11 LCD_PWM	LCD_PWM
5,11 TFT_CLK	TFT_CLK
5,11 HSYNC	HSYNC
5,11 VSYNC	VSYNC
5,11 DE	DE
5,11 LCD_R[7..3]	LCD_R[7..3]
5,11 LCD_G[7..2]	LCD_G[7..2]
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IO电平1.8V

FPGA/IO 141+30



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CONN		
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