

Block Diagram

NOTES:

[illegible]

PAGES	DESCRIPTION
0	Title, Note, Block Diagram, Revision History
1	POWER
2	CLOCK
3	USB_HS
4	ARM
5	FPGA
6	ETH
7	SDRAM
8	DDR2
9	RS-485/RS-422/RS-232/CAN
A	LCD
B	CONNECTOR
C	-----
D	-----
E	-----
F	-----
10	-----
11	-----
12	-----
13	-----

Engineer: -----

Engineer: W XK

GINGKO

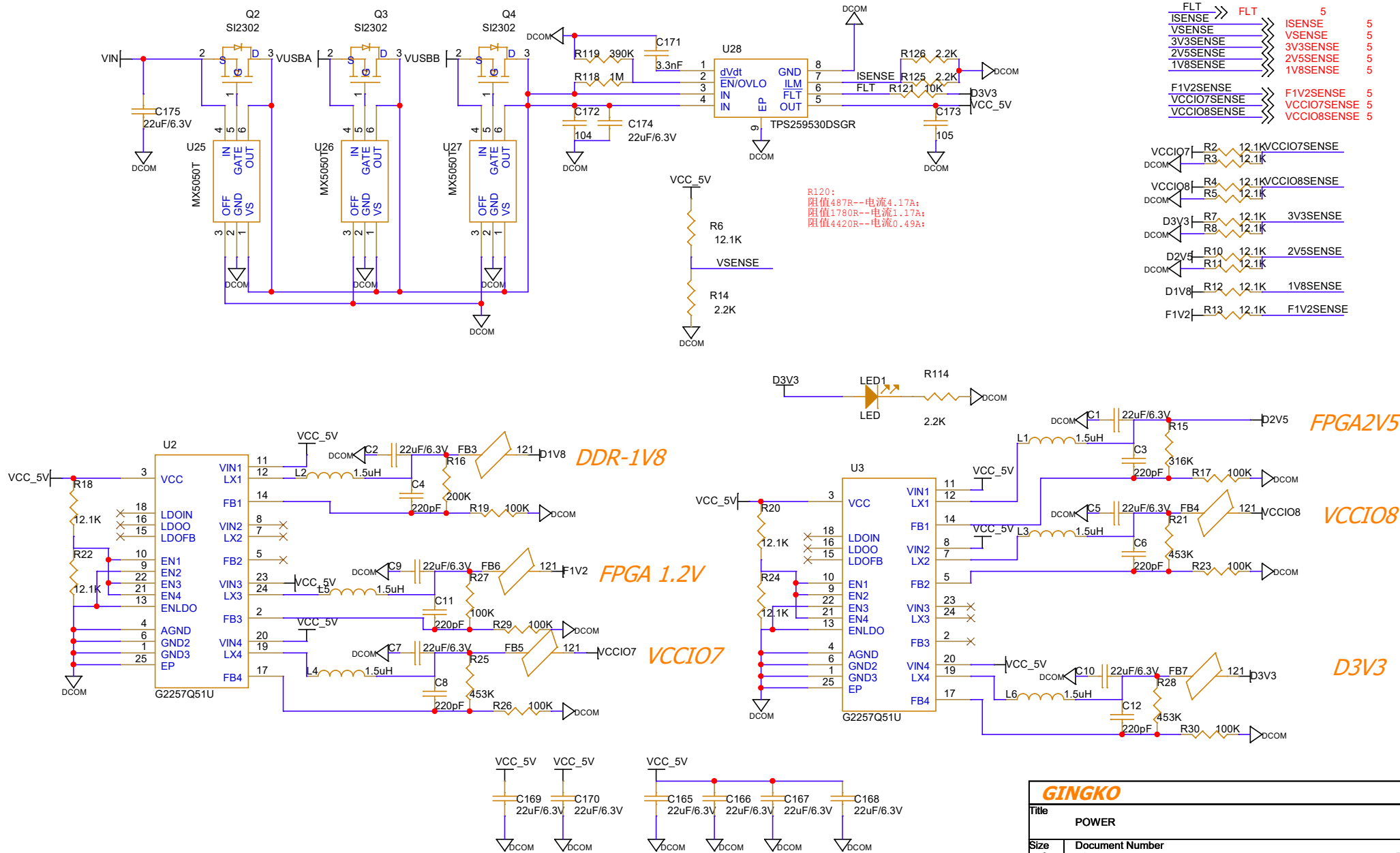
Title
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Size B	Document Number 0_Title
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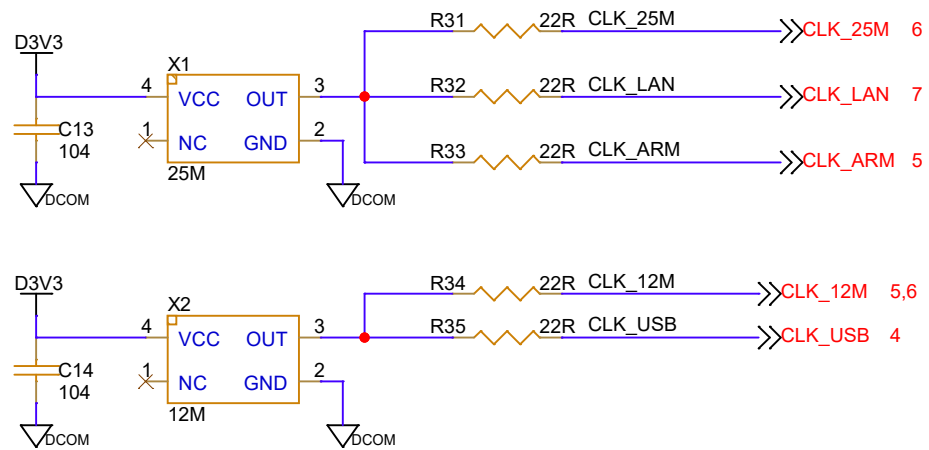
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Date: Monday, July 24, 2023

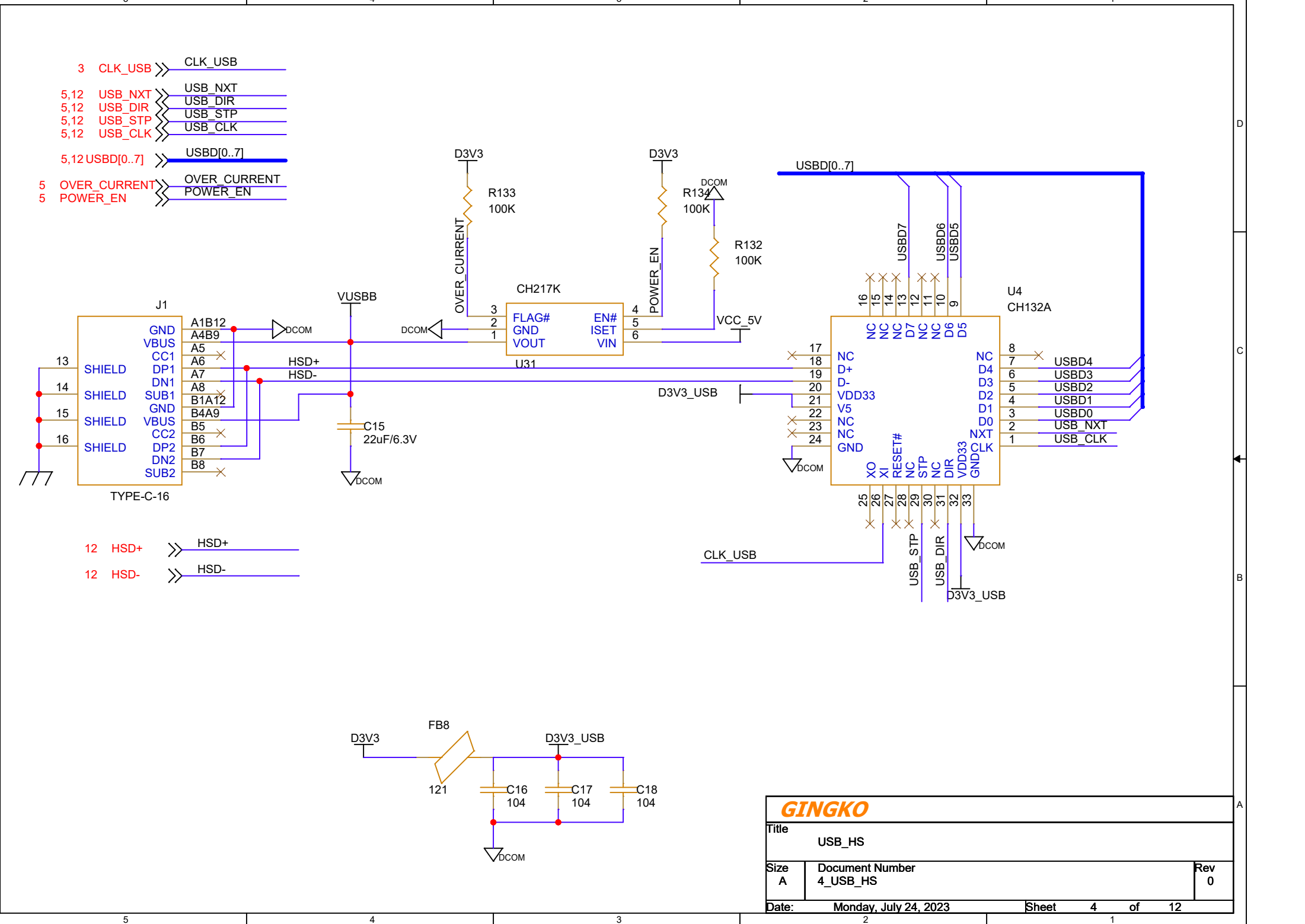
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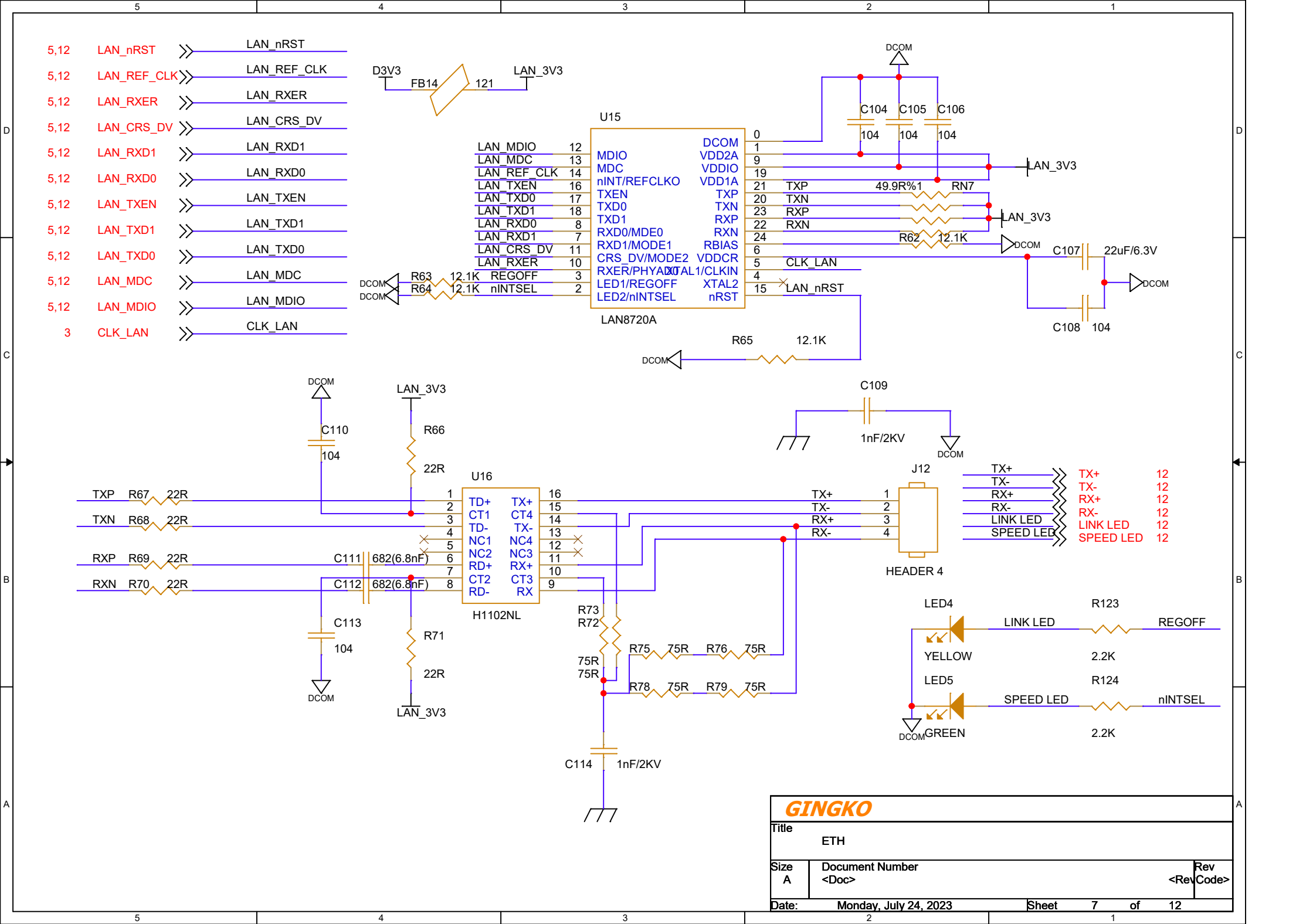


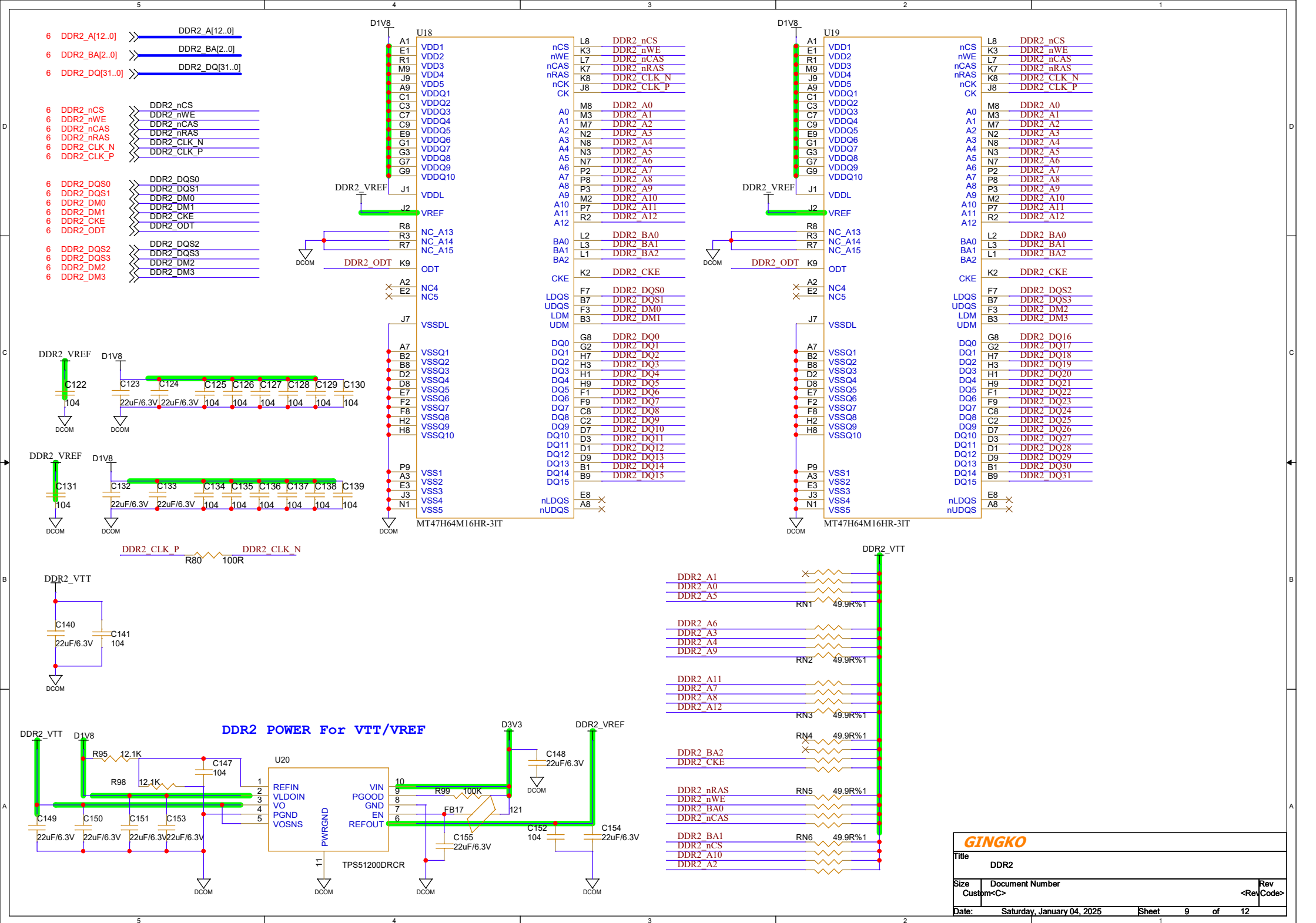
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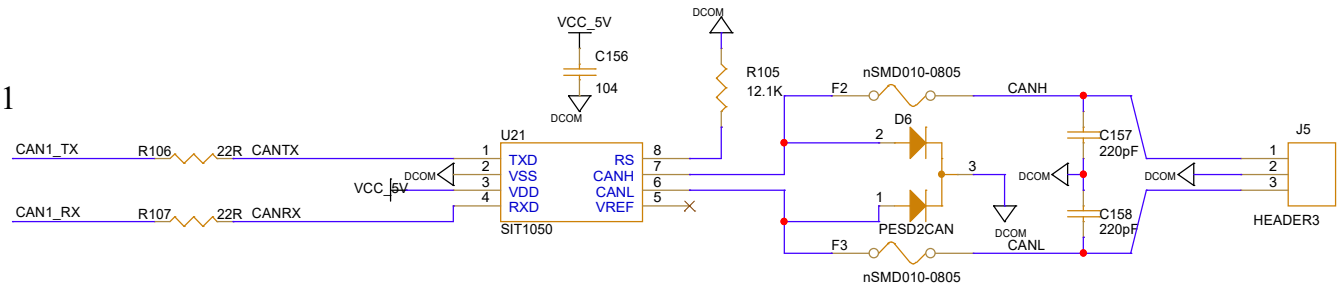
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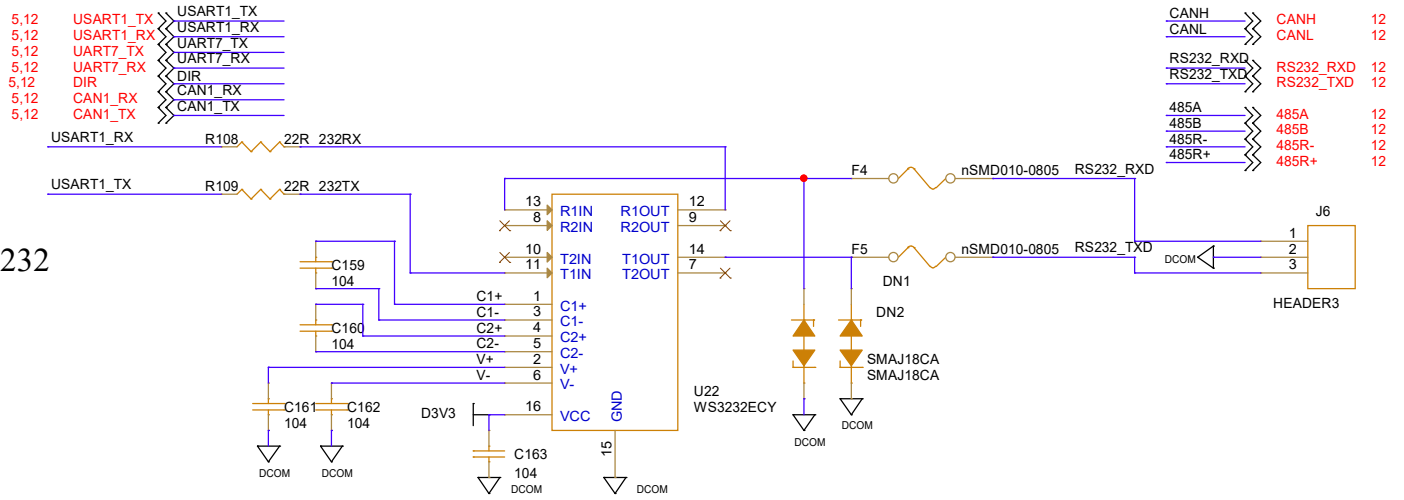




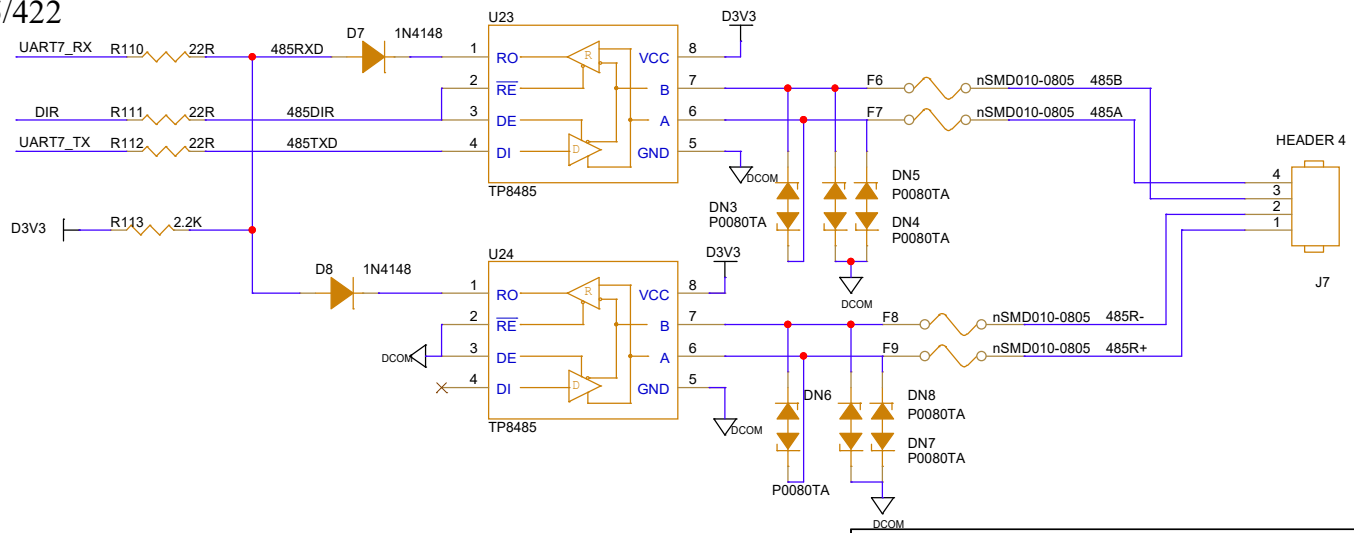
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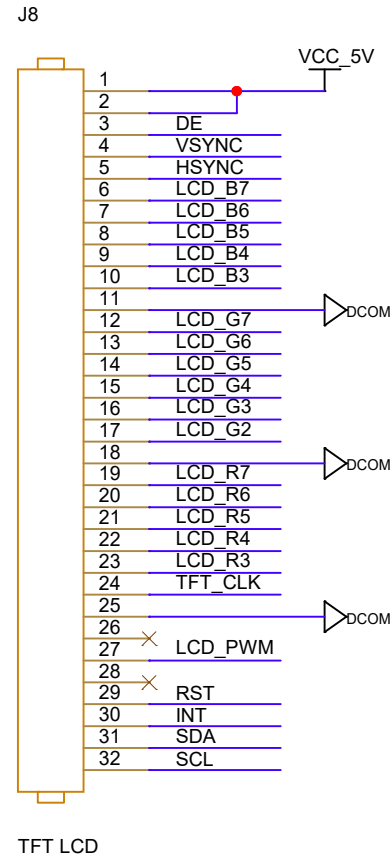
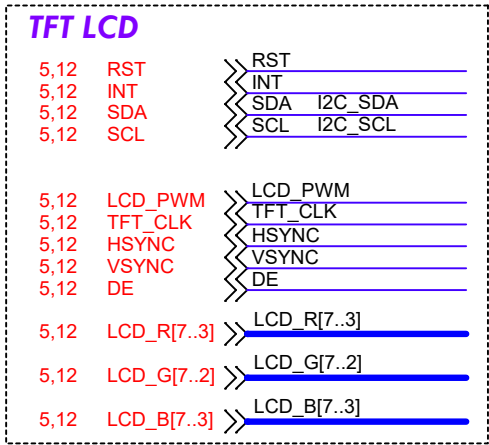
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485/422

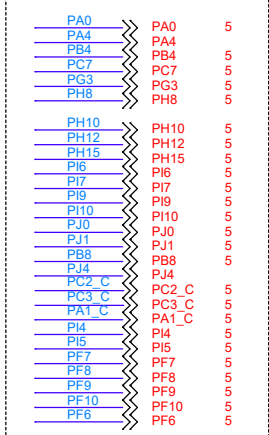


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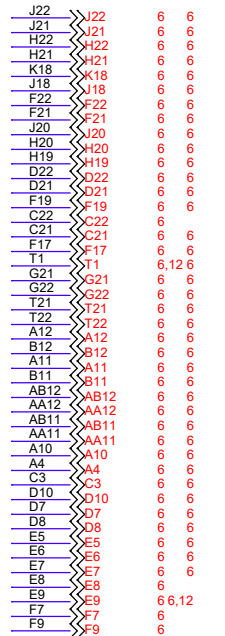
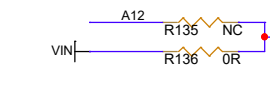
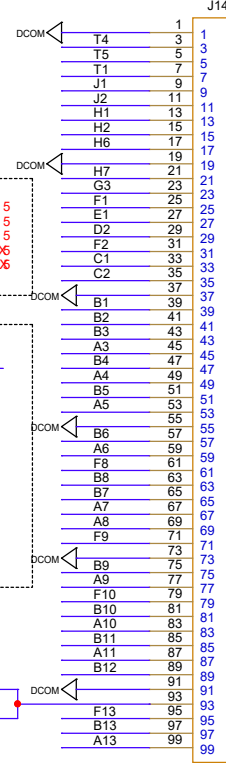
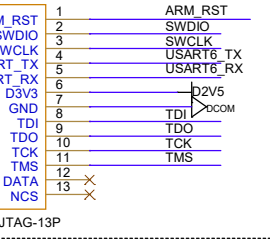
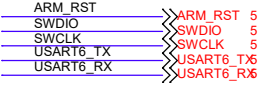
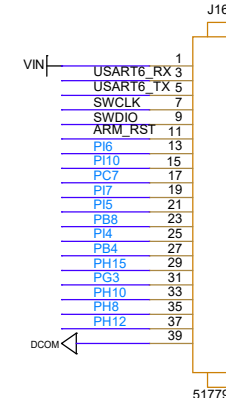
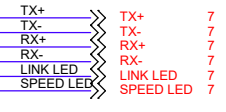
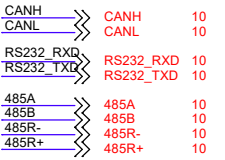
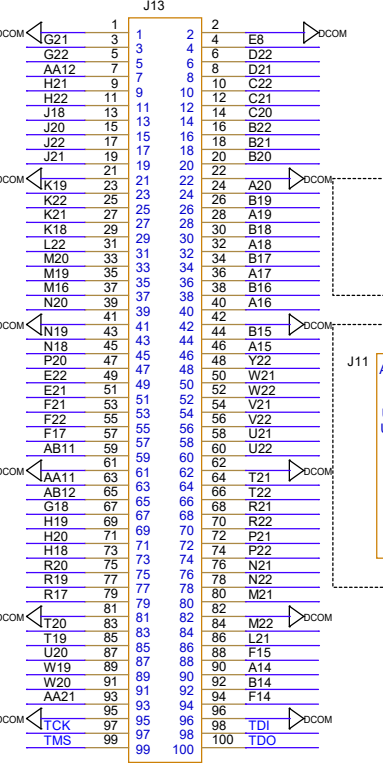
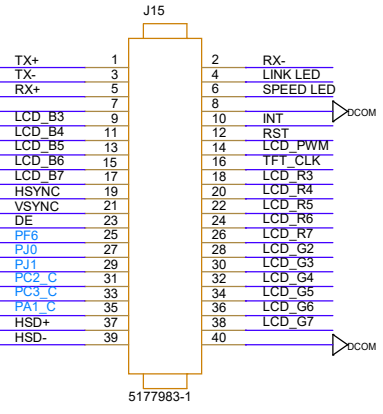
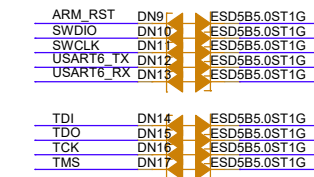
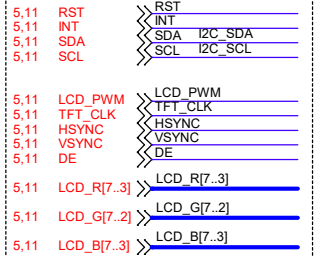


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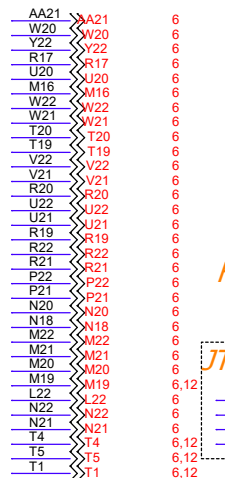
ARM IO 27



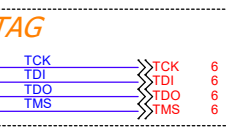
TFT LCD



IO电平1.8v



FPGA/IO 141+30



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CONN			
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