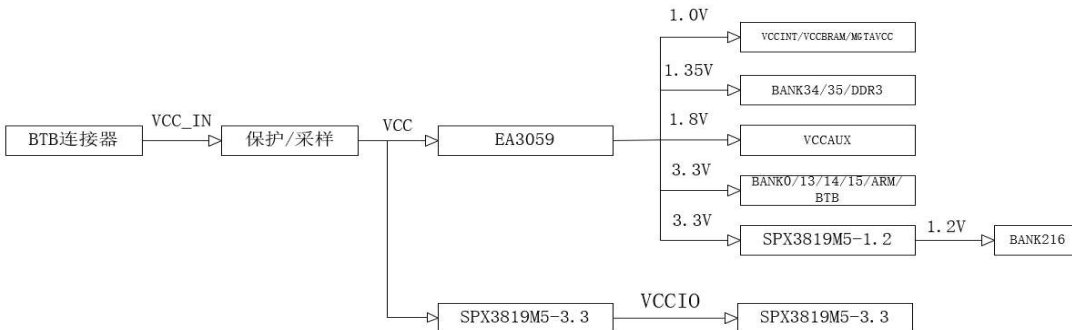


Block Diagram



NOTES:

- 1.增加0R电阻;
- 2.FPGA晶振引脚调整到B13_L12N;
- 3.ARM的LDO供电引脚改为1.8V;

[illegible]

PAGES	DESCRIPTION
0	Title, Note, Block Diagram, Revision History
1	POWER
2	CLOCK
3	FPGA
4	ARM
5	SDRAM
6	DDR3
7	CONN
8	-----
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A	-----
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F	-----
10	-----
11	-----
12	-----
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Engineer: -----

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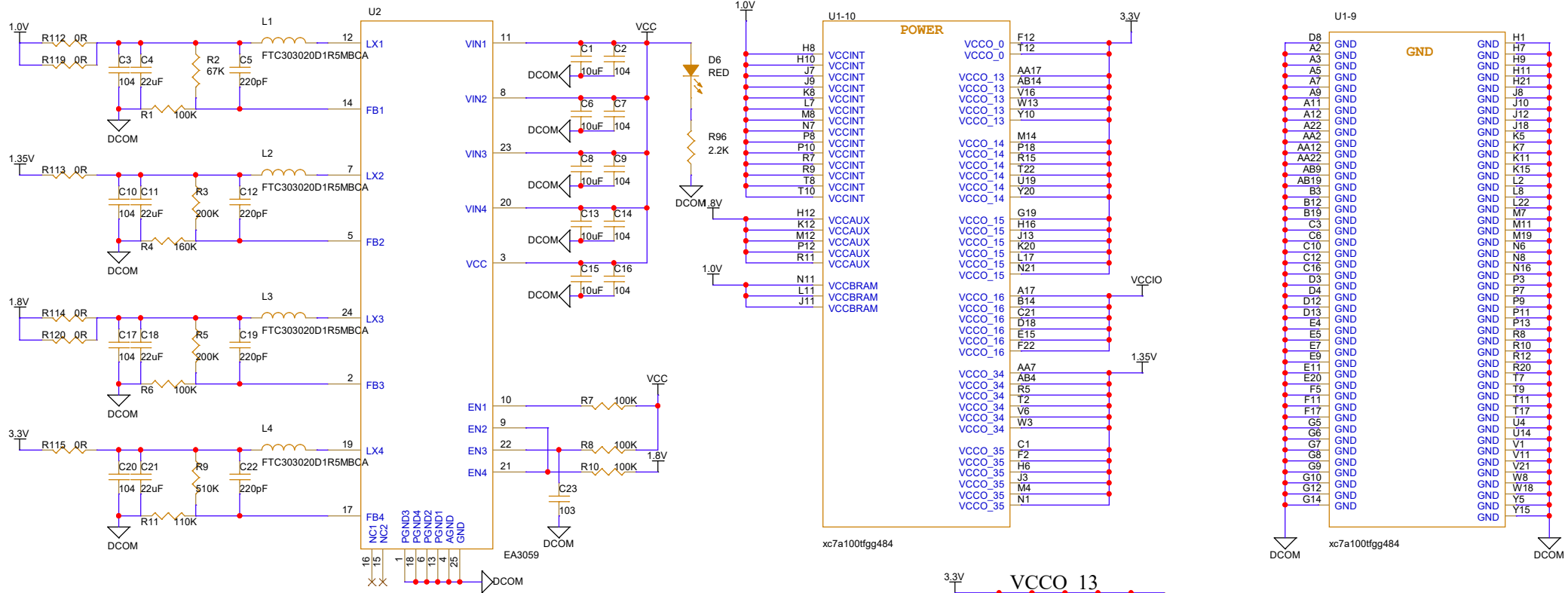
Title	GT7000
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Size	Document Number
B	0 Title

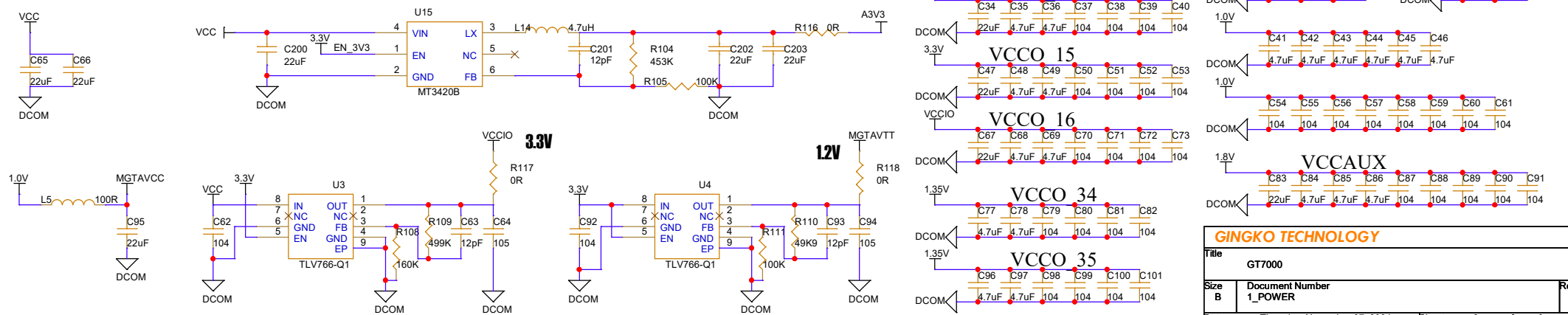
Date: Thursday, November 07, 2024 Sheet 1 of 8

Date: Thursday, November 07, 2024 Sheet 1 of 8

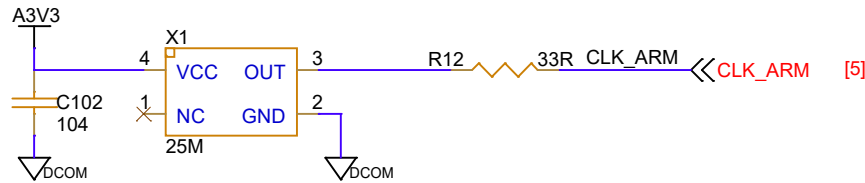
$$V_{out}=0.6 \cdot R1/R2+0.6$$



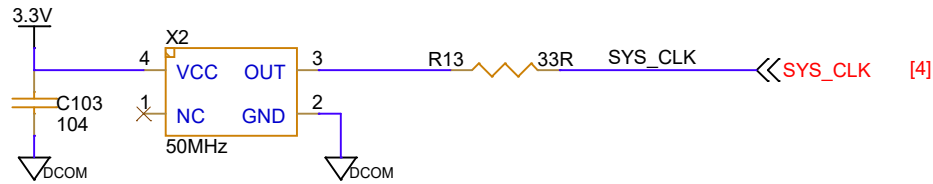
Power On Sequence:
1.0V -> 1.8V -> 1.35V & 3.3V -> VCCIO



ARM



FPGA-SYS



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Title GT7000			
Size A	Document Number 2_CLK		Rev 0
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