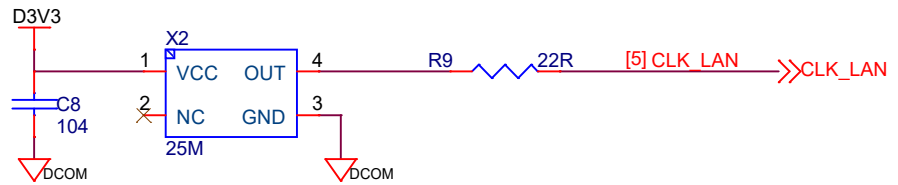
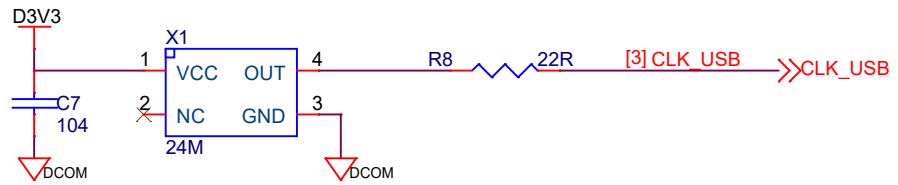
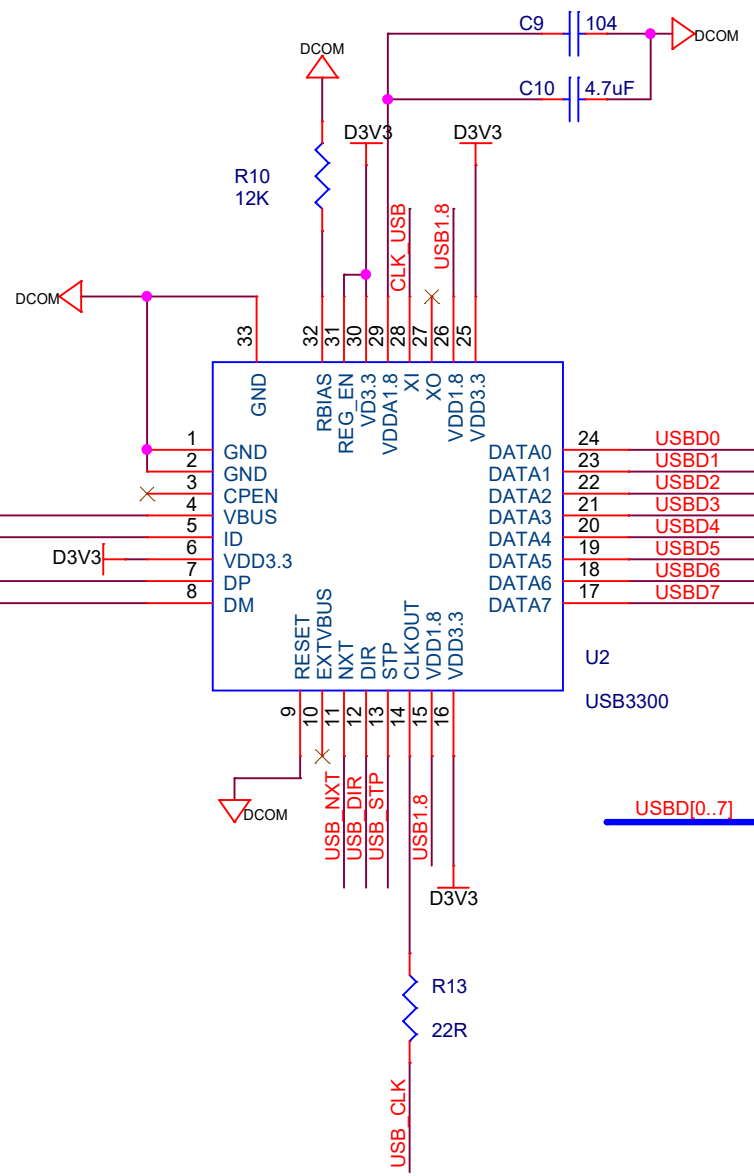
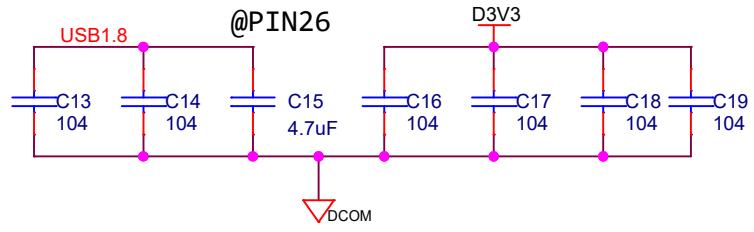
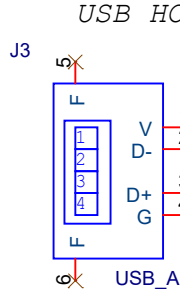
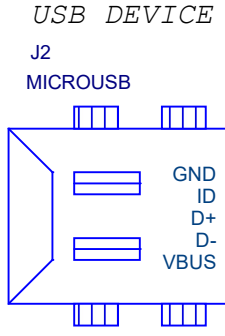
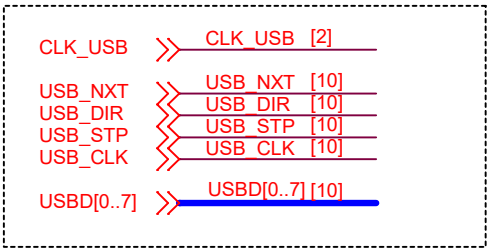


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Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Wednesday, February 26, 2020	Sheet 1 of 11



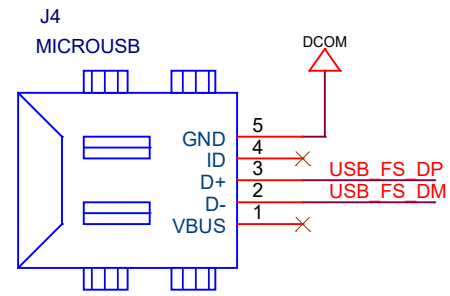
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Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Wednesday, February 26, 2020	Sheet 2 of 11



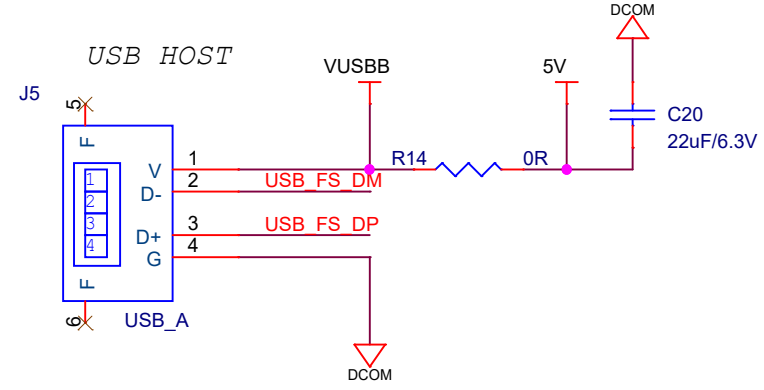
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Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Wednesday, February 26, 2020	Sheet 3 of 11

USB\_FS\_DP >> USB\_FS\_DP [10]  
 USB\_FS\_DM >> USB\_FS\_DM [10]

USB DEVICE

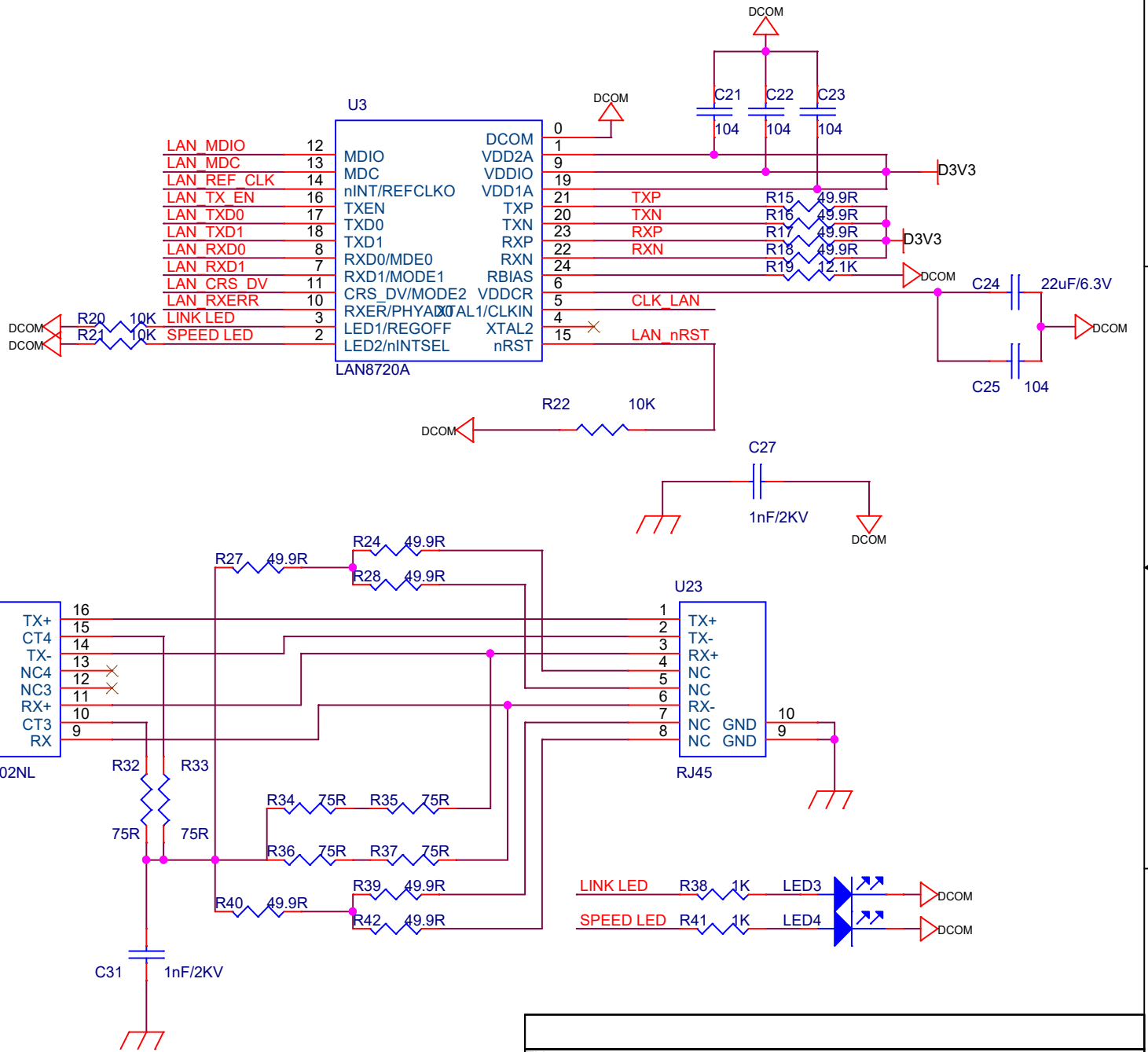


USB HOST

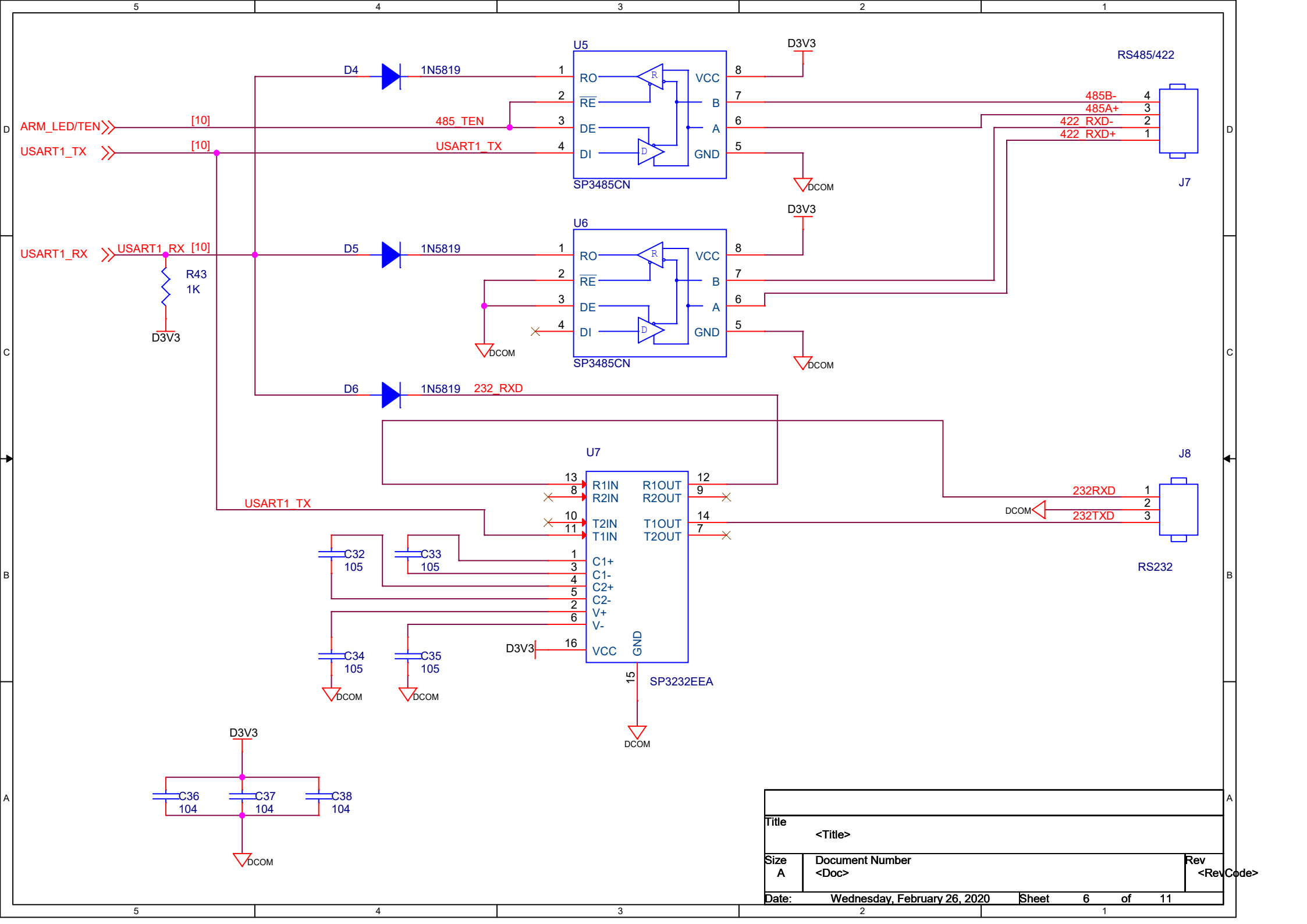


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Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Wednesday, February 26, 2020	Sheet 4 of 11

LAN_nRST	LAN_nRST	[10]
LAN_REF_CLK	LAN_REF_CLK	[10]
LAN_RXERR	LAN_RXERR	[10]
LAN_CRSDV	LAN_CRSDV	[10]
LAN_RXD1	LAN_RXD1	[10]
LAN_RXD0	LAN_RXD0	[10]
LAN_TX_EN	LAN_TX_EN	[10]
LAN_TXD1	LAN_TXD1	[10]
LAN_TXD0	LAN_TXD0	[10]
LAN_MDC	LAN_MDC	[10]
LAN_MDIO	LAN_MDIO	[10]
CLK_LAN	CLK_LAN	[2]

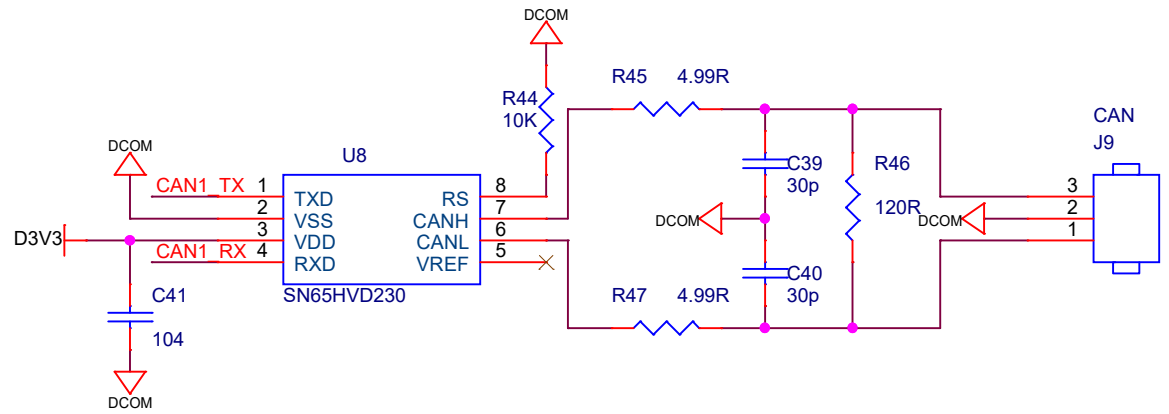


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Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Wednesday, February 26, 2020	Sheet 5 of 11

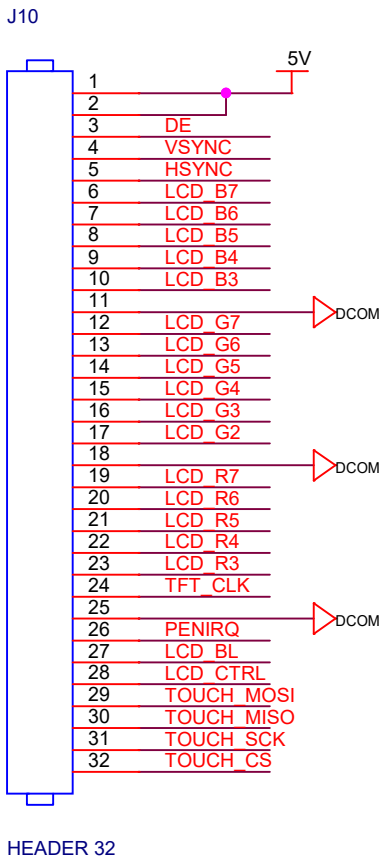
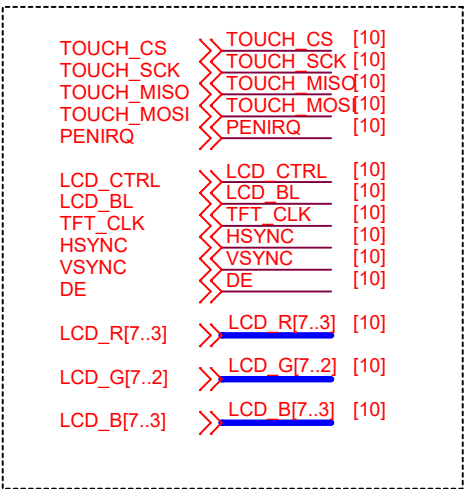


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Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Wednesday, February 26, 2020	Sheet 6 of 11

CAN1\_TX >>> CAN1\_TX [10]  
 CAN1\_RX >>> CAN1\_RX [10]

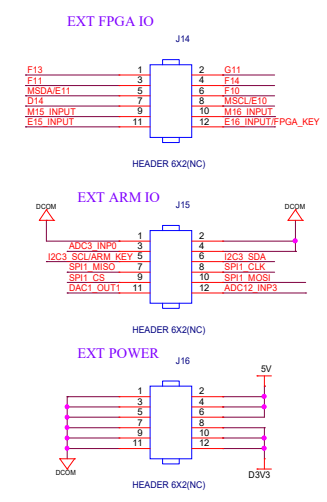
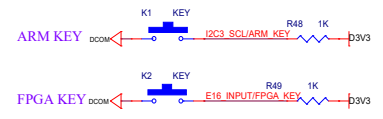
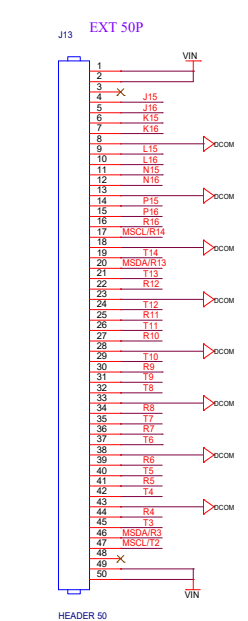
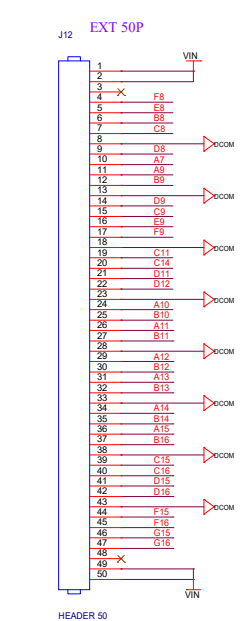
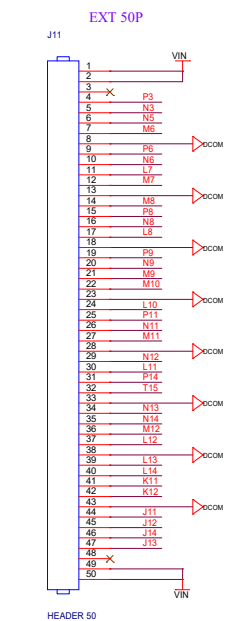
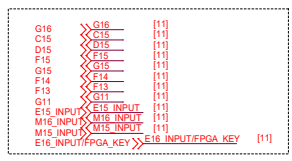
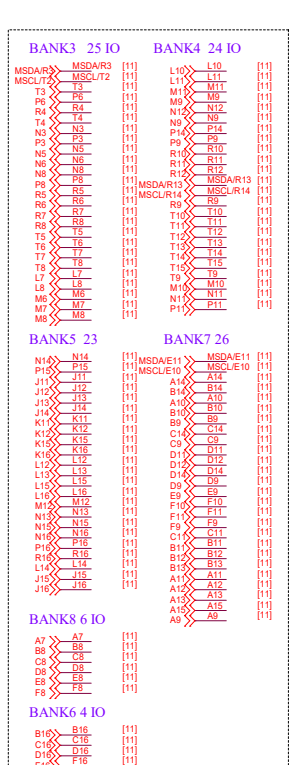


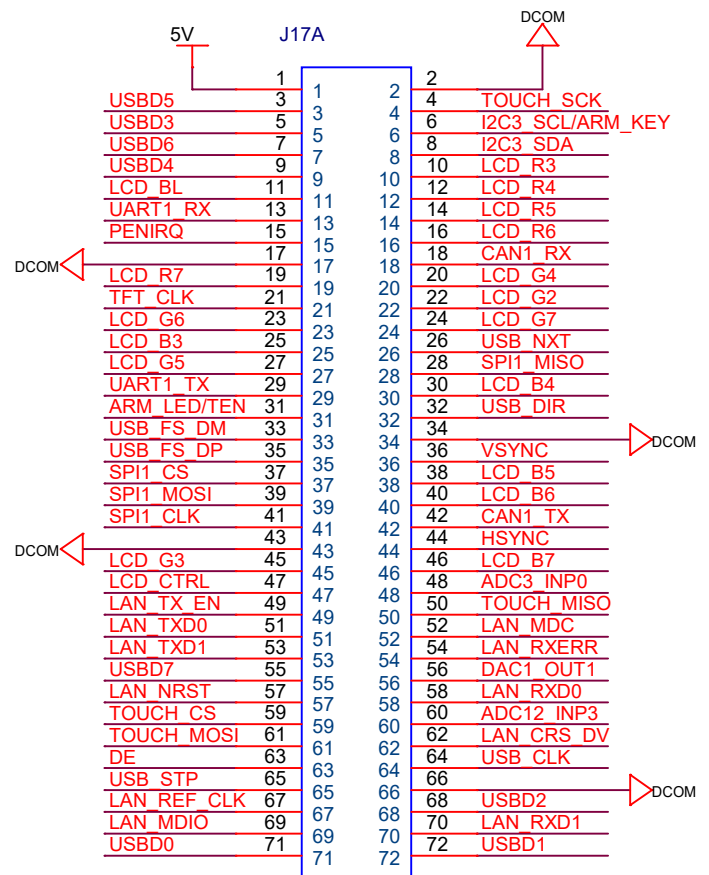
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Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Wednesday, February 26, 2020	Sheet 7 of 11



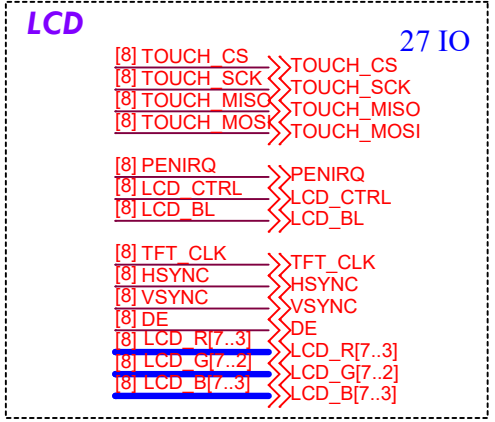
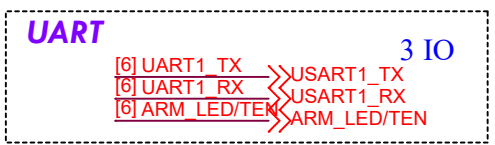
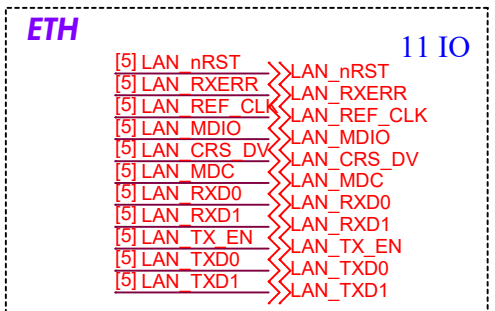
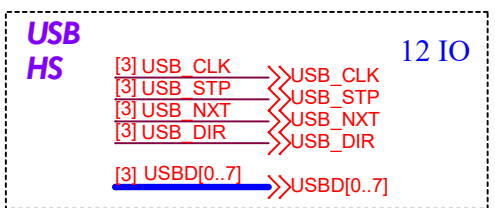
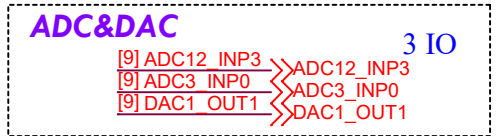
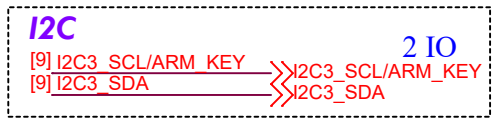
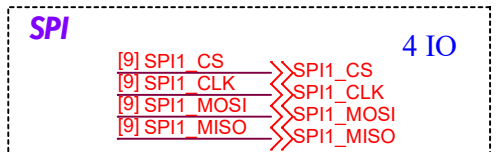
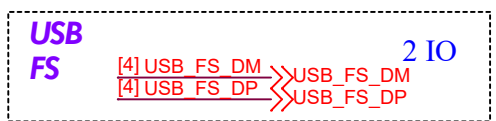
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Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Wednesday, February 26, 2020	Sheet 8 of 11







GOLDFINGER



Title		
<Title>		
Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Wednesday, February 26, 2020	Sheet 10 of 11



P\_OUT

DCOM

J17B

J17C

BANK3 25 IO

BANK4 24 IO

BANK8 6 IO

73	73	74	74	
MSCL/T2	75	76	76	P3
MSDA/R3	77	78	78	N3
T3	79	80	80	N5
R4	81	82	82	M6
T4	83	84	84	P6
R5	85	86	86	N6
T5	87	88	88	L7
R6	89	90	90	M7
T6	91	92	92	M8
	93	94	94	
DCOM	R7	95	96	P8
	T7	97	98	N8
	R8	99	100	L8
	T8	101	102	P9
	T9	103	104	N9
	R9	105	106	M9
	T10	107	108	M10
	R10	109	110	L10
	T11	111	112	P11
	R11	113	114	N11
DCOM		115	116	
	T12	117	118	M11
	R12	119	120	N12
	T13	121	122	L11
	MSDA/R13	123	124	P14
	T14	125	126	T15
	MSCL/R14	127	128	N13
	R16	129	130	N14
	P16	131	132	M12
	P15	133	134	L12
	N16	135	136	L13
DCOM		137	138	
	N15	139	140	L14
	M16 INPUT	141	142	K11
	M15 INPUT	143	144	K12
	L16	145	146	J11
	L15	147	148	J12
	K16	149	150	J14
	K15	151	152	J13
	J16	153	154	G11
	J15	155	156	F13
	G16	157	158	F14
DCOM		159	160	

G15	161	162	162	F11
F16	163	164	164	F10
F15	165	166	166	MSDA/E11
E16 INPUT/FPGA_KEY	167	168	168	MSCL/E10
E15 INPUT	169	170	170	D14
D16	171	172	172	D12
D15	173	174	174	D11
C16	175	176	176	C14
C15	177	178	178	C11
B16	179	180	180	F9
	181	182	182	
DCOM	A15	183	184	E9
	B14	185	186	C9
	A14	187	188	D9
	B13	189	190	B9
	A13	191	192	A9
	B12	193	194	F8
	A12	195	196	E8
	B11	197	198	B8
	A11	199	200	C8
	B10	201	202	D8
	A10	203	204	A7

GOLDFINGER

[9] MSDA/R3	MSDA/R3
[9] MSCL/T2	MSCL/T2
[9] T3	T3
[9] P6	P6
[9] R4	R4
[9] T4	T4
[9] N3	N3
[9] P3	P3
[9] N5	N5
[9] N6	N6
[9] N8	N8
[9] P8	P8
[9] R5	R5
[9] R6	R6
[9] R7	R7
[9] R8	R8
[9] T5	T5
[9] T6	T6
[9] T7	T7
[9] T8	T8
[9] L7	L7
[9] L8	L8
[9] M6	M6
[9] M7	M7
[9] M8	M8

[9] L10	L10
[9] L11	L11
[9] M11	M11
[9] M9	M9
[9] N12	N12
[9] N9	N9
[9] P14	P14
[9] P9	P9
[9] R10	R10
[9] R11	R11
[9] R12	R12
[9] MSDA/R13	MSDA/R13
[9] MSCL/R14	MSCL/R14
[9] R9	R9
[9] T10	T10
[9] T11	T11
[9] T12	T12
[9] T13	T13
[9] T14	T14
[9] T15	T15
[9] T9	T9
[9] M10	M10
[9] N11	N11
[9] P11	P11

[9] A7	A7
[9] B8	B8
[9] C8	C8
[9] D8	D8
[9] E8	E8
[9] F8	F8

BANK6 14 IO

[9] B16	B16
[9] C16	C16
[9] D16	D16
[9] F16	F16
[9] G16	G16
[9] C15	C15
[9] D15	D15
[9] F15	F15
[9] G15	G15
[9] F14	F14
[9] F13	F13
[9] G11	G11
[9] E15 INPUT	E15_INPUT

[9] E16 INPUT/FPGA\_KEY >>> E16\_INPUT/FPGA\_KEY

BANK5 25

BANK7 26

[9] N14	N14
[9] P15	P15
[9] J11	J11
[9] J12	J12
[9] J13	J13
[9] J14	J14
[9] K11	K11
[9] K12	K12
[9] K15	K15
[9] K16	K16
[9] L12	L12
[9] L13	L13
[9] L15	L15
[9] L16	L16
[9] M12	M12
[9] N13	N13
[9] N15	N15
[9] N16	N16
[9] P16	P16
[9] R16	R16
[9] L14	L14
[9] J15	J15
[9] J16	J16
[9] M15 INPUT	M15_INPUT
[9] M16 INPUT	M16_INPUT

[9] MSDA/E11	MSDA/E11
[9] MSCL/E10	MSCL/E10
[9] A14	A14
[9] B14	B14
[9] A10	A10
[9] B10	B10
[9] B9	B9
[9] C14	C14
[9] C9	C9
[9] D11	D11
[9] D12	D12
[9] D14	D14
[9] D9	D9
[9] E9	E9
[9] F10	F10
[9] F11	F11
[9] F9	F9
[9] C11	C11
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GOLDFINGER

Title		
<Title>		
Size	Document Number	Rev
A	<Doc>	<RevCode>
Date:	Wednesday, February 26, 2020	Sheet 11 of 11